No. 15-1091

United States Court of Appeals for the Federal Circuit

MCM PORTFOLIO LLC,
APPELLANT,

v.

HEWLETT-PACKARD COMPANY,
APPELLEE.

APPEAL FROM PATENT AND TRADEMARK OFFICE –
PATENT TRIAL AND APPEAL BOARD IN NO. IPR2013-00217

PRINCIPAL BRIEF FOR APPELLANT MCM PORTFOLIO LLC

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Attorneys for Appellant

Dated: January 20, 2015

CERTIFICATE OF INTEREST

1. The full name of every party represented by me:

   MCM Portfolio LLC

2. Other real parties in interest represented by me:

   None

3. All parent corporations and any publicly held companies that own 10 percent or more of the stock of the party or amicus curiae represented by me are:

   None

4. The names of all the firms or lawyers that appeared for MCM Portfolio LLC in the *Inter Partes* Review and who are expected to appear in this case:

   Edward P. Heller III and Susan L. Anhalt

   /s/ Edward P. Heller III
   Edward P. Heller III

Dated: January 20, 2015

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STATEMENT OF RELATED CASES

In re MCM Portfolio LLC, No. 2014-104, was a *mandamus* petition in the present case regarding the Patent Trial and Appeal Board's decision to institute an *inter partes* review of US patent 7,162,549.

Technology Properties Limited LLC v. Action Electronic Co., et al., No. 2:11-cv-00372-TJW (E.D. Tex. 2011) is a complaint for patent infringement of US patent 7,162,549 served on Pandigital, Inc. on October 5, 2011.

Certain Digital Photo Frames and Image Display Devices and Components Thereof, Investigation, No. 337-TA-807, instituted on September 27, 2011, resulted in a limited exclusion order against Pandigital, Inc. 78 Fed. Reg. 16707-9 (March 18, 2013) (Exclusion order directed to Digital Photo Frames that infringe claims 1, 7, 11, 17, 19 and 21 of US patent 7,162,549.)

US patent application number 12/351,691, is a pending reissue of US patent 7,162,549.

JURISDICTIONAL STATEMENT

The Board had statutory jurisdiction under 35 U.S.C. §§ 311-319 to consider the request for *inter partes* review in the Petition filed by Hewlett-Packard Company on March 27, 2013. The Board did not have subject matter jurisdiction to initiate the *inter partes* review of US 7,162,549 or enter a final written decision pursuant to 35 U.S.C. § 318(a). This court has statutory jurisdiction of this matter under 35 U.S.C. §§ 319 and 141 and 28 U.S.C. § 1295(a)(4)(A). The decisions and orders from which the present appeal is taken are final. A notice of appeal was timely filed on October 6, 2014.

STATEMENT OF ISSUES

This appeal challenges the determinations made by the Patent Trial and Appeal Board in its decision to institute an *inter partes* review of US 7,162,549 and in its final written decision on the following issues:

1. Whether the Petition requesting *inter partes* review of US 7,162,549 filed by Hewlett-Packard Company established by a preponderance of the evidence as required under 35 U.S.C. § 316(e) that claims 7, 11, 19 and 21 are unpatentable;

2. Whether Hewlett-Packard Company established it had standing to file the Petition and whether 35 U.S.C. § 315(b) barred the institution of the *inter partes* review under existing law on privity; and

3. Whether actions to cancel or revoke a patent must be tried in Article III Courts with access to a jury under the Seventh Amendment to the United States Constitution.

STATEMENT OF THE CASE

This is an appeal from the final written decision of the Patent Trial and Appeal Board ("Board") pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73 in IPR 2013-00217 regarding US patent 7,162,549 ("US '549") which found that claims 7, 11, 19 and 21 of US '549 were unpatentable and which denied MCM Portfolio LLC's ("MCM") assertion that a patent owner is entitled under the Seventh Amendment of the Constitution to have the revocation or cancellation of its patent tried by an Article III Court with access to a jury. This appeal is also an appeal from the Board's institution order in which the Board inappropriately initiated an *inter partes* review of claims 7, 11,

19 and 21 of US '549 when Hewlett-Packard Company lacked standing to request the review and the review was barred by 35 U.S.C. § 315(b).

Hewlett-Packard Company ("HP") filed a petition (the "Petition") requesting *inter partes* review ("IPR") of US '549 on March 27, 2013, alleging the unpatentability of claims 7, 11, 19 and 21. Patent owner MCM filed a preliminary response on June 27, 2013, establishing that the Petition had not presented facts sufficient to show there was a reasonable likelihood that HP would prevail on at least one of the claims challenged and therefore Petitioner HP had not met its statutory burden of proof under 35 U.S.C. § 314(a). MCM's preliminary response further established that HP lacked standing to request the IPR and that the institution of the IPR was barred by 35 U.S.C. § 315(b) because Pandigital, Inc., a company served with a complaint for infringement of US '549 more than a year prior to the filing date of HP's Petition, was HP's privy at the time. On September 10, 2013, the Board ordered the institution of the IPR. On September 24, 2013, MCM requested a rehearing on the § 315(b) privy issue based on this court's intervening opinion in *Aevoe Corp. v. AE Tech Co., Ltd.*, 727 F.3d 1375 (Fed. Cir. 2013). On October 10, 2013, the Board denied MCM's rehearing

request. On October 24, 2013, MCM requested *mandamus* of this court on the § 315(b) privy issue. On February 18, 2014, this court denied *mandamus* without prejudice to raising the issue on appeal from a final written decision.[1] MCM filed its patent owner's response to the Petition on December 9, 2013, again establishing that HP had not proven a *prima facie* case of invalidity of the challenged claims, and that the Board lacked subject matter jurisdiction to revoke or cancel a patent. Oral arguments were heard on June 4, 2014. The Board issued its final written decision on August 6, 2014 (the "Decision"), determining claims 7, 11, 19 and 21 unpatentable and denying MCM's challenge to the Board's jurisdiction. MCM timely filed a notice of appeal on October 6, 2014.

[1] MCM sought a *writ of mandamus* (No. 14-104) on the Board's institution of the IPR, which this Court denied without prejudice to MCM's § 315(b) arguments. ("We deny the petition without prejudice to MCM attempting to raise its section 315(b) arguments on appeal after final decision by the Board.")

STATEMENT OF THE FACTS

A. HP's Petition Did Not Prove Unpatentability of The Claimed Controller Chip of US '549

1. Petitioner Has The Burden of Proving Unpatentability

In 2011 Congress passed the America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) which among other things created the *inter partes* review process otherwise known as an IPR, set forth in 35 U.S.C. §§ 311-319. The process is initiated by the filing of a petition which, under 35 U.S.C § 312(a)(3), must identify "with particularity" each claim challenged, the grounds on which the challenge to each claim is based, and the evidence that supports the grounds for the challenge to each claim. The patent owner is given an opportunity to file a preliminary response (§ 313) after which the director determines whether the petition "shows there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a). If that determination is made, a "trial" is instituted and the patent owner is entitled to file a response, to which the petitioner may reply. Section 316(e) mandates that the petitioner "shall have the burden of proving a proposition of

unpatentability." Thereafter there is oral argument, and then a final written decision. The evidence to support a final written decision of unpatentability must be found in the petition when the Board does not rely on evidence in the response, as is the present case.

2. The Claims of US '549 At Issue

The claims at issue are directed to a controller chip that has three distinct structures: an interface mechanism, a detector and a flash adapter. The inventors of US '549 designed a controller chip that is specifically adapted to read multiple types of flash cards (otherwise referred to in the claims as flash storage systems), and, significantly, to read flash cards that have controllers for error correction and also to read flash cards that do not have controllers for error correction. A271, Abstract; A322; claims 7 and 11. The US '549 controller chip was specifically designed to be located on a flash card reader. *Ibid.* Nor does the US '549 controller chip need to have a duplicate controller on the flash cards that have controllers in order to function reliably. In fact, the controller chip disclosed in US '549 *cannot* be used on a flash card – it can only be used in a reader.

The US '549 controller chip *includes* a detector to determine whether a flash card (the claims use the term flash storage systems) has a controller for error correction or not and, in the event that the flash card does not have a controller for error correction, performs in firmware the necessary error correction, including managing bad block mapping of the flash section of the flash card. A322; claims 7 and 11. The claimed controller chip detector detects the difference between multiple types of flash cards without using a mechanical/optical detector or a switch, or requiring that the flash cards themselves have visible characteristics such as physical casing differences (a notch in one side) in order to determine whether the flash card has a controller for error correction.

Thus the claims of US '549 require a controller *chip* that has three distinct structures:

- an **interface mechanism** capable of receiving flash storage systems with controller and controllerless flash storage systems; A322:30:54-57;
- a **detector** to determine whether the flash storage system includes a controller for error correction; A322:30:57-59; and

- **a flash adapter** which comprises firmware to perform, *in an event* where the flash storage system does not have a controller for error correction, operations to manage error correction of the flash section, including bad block mapping of the flash section in the flash storage system that is coupled to the flash adapter section. A322:30:59-65.

The claimed controller chip in US '549 is specifically adapted to be located on flash card readers that read multiple types of flash cards allowing the card reader to read a variety of flash cards, none of which employ the same controller as the claimed controller chip. E.g., Fig. 6, controller 40, A280. The claimed controller chip is specifically adapted to read flash cards that do not have error correction controllers. A321:28:6-14. The claimed controller chip is a function of the card reader only and has no reliance on the same controller or controller chip being on the flash card, nor can it be adapted for use on a flash card. The claimed controller chip detects the presence of an error correction controller on a flash card and adapts itself through firmware accordingly to provide error correction in the absence thereof. A312:10:52-62; A321:28:42-43; A321:28:51-A322:29:6. The claimed

controller chip is specifically designed for use on flash card readers. *Ibid.*

3. HP's References – Kobayashi and Kikuchi

HP's Petition alleged invalidity of independent claims 7 and 11, and claims 19 and 21 depending from claims 7 and 11 respectively. A44. The Board instituted the IPR, and ultimately invalidated the claims, based on a combination of Kobayashi and Kikuchi, A29, which, even together, do not disclose the structural limitations of US '549. In fact, neither of HP's references disclose a controller chip with any of US '549 claim controller chip structures.

Kobayashi discloses a *reader* having a variety of controllers, selector switches and mechanical/optical detectors. E.g., Fig. 11, reader 12, conversion controller 122, ATA controller 124, selector 134, detector 133. A334. Kobayashi does not disclose a controller chip having *any* of the claimed controller chip structural limitations. HP's Petition, however, inaccurately alleged that Kobayashi generally disclosed *all* of the limitations of the claims but for one: the management of bad block mapping in firmware in the event a flash card did not have a controller for error correction. For that "function," HP relied upon Kikuchi. A9:2-

4. HP's Petition blatantly ignored, however, that the bad block mapping functionality incorporated into Kobayashi to meet the claims was required to be incorporated into the flash adapter of a controller chip that also has an interface mechanism, as claimed, and a detector, as claimed.

Kobayashi's *reader* 12 has a conversion controller 122 that can *only* communicate with ATA controllers. A338:6:1222. Kobayashi's ATA controller 124 is alternatively located on the reader 12 or on a flash card 13. A341:12:43-46. The presence of a physical notch in the card casing indicates whether a card has this ATA controller or not. A342:13:11-12. (Card notch shown in Fig. 11 in lower right card.) The reader 12 employs a mechanical/optical detector 133, not a controller, to determine what kind of flash card is present by detecting the notch in the card. A341:12:67-A342:13:2; A342:13:12-13. A switch 134 selects one of the two controllers depending on the type of flash card present. A342:13:2-8.

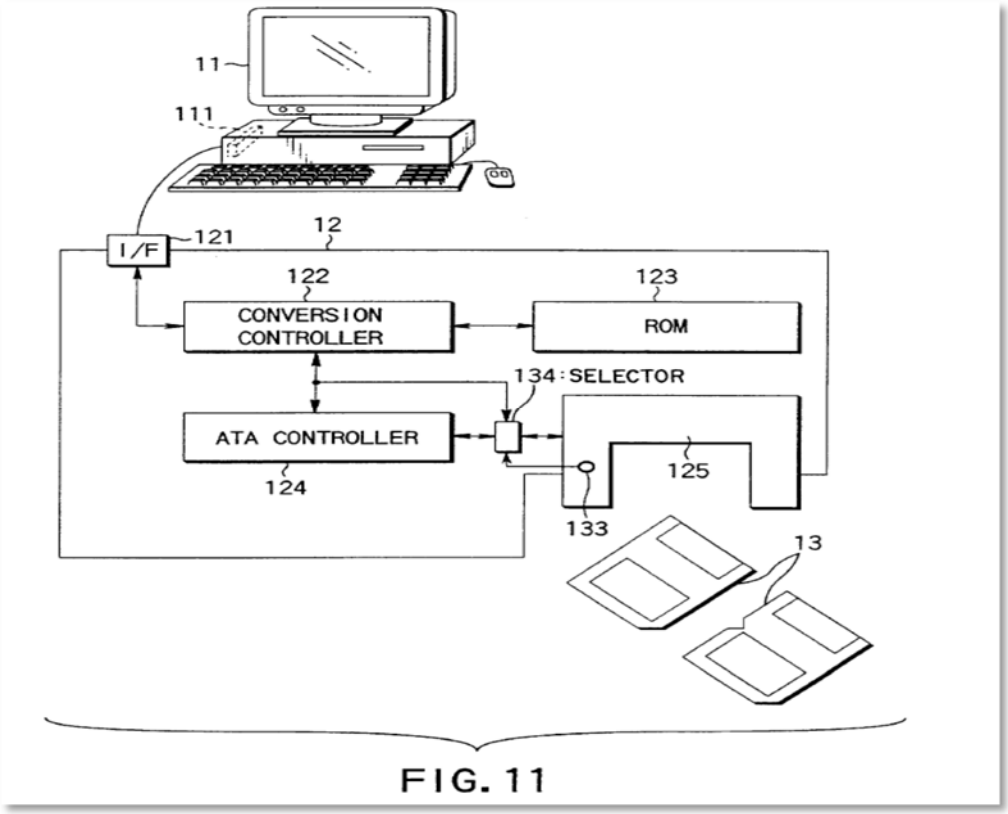

FIG. 11

Quite simply, Kobayashi discloses no controller chip that interfaces with both flash cards that have controllers and flash cards that do not. Kobayashi discloses no controller chip that has a detector for determining whether a card has a controller, let alone a controller for error correction as claimed. Kobayashi discloses no controller chip that manages bad block mapping of the flash card in the event that a flash card does not have a controller for error correction. Kobayashi discloses no controller chip that is capable of receiving both flash storage systems with controllers and controllerless flash storage systems as claimed. Kobayashi discloses no controller chip that has any

of the claimed structures of US '549, let alone all the claimed structures.

At most, Kobayashi discloses a *reader* that contains a mechanical optical detector that is limited to detecting physical differences in the casings of flash cards (i.e., it detects that there either is or is not a "notch" cut out of the plastic casing on the side of the flash card) that functions *so long as* there is the same ATA controller in both the reader and on the flash card that have controllers.

Most importantly, Kobayashi contains no disclosure on how to detect whether a flash card has an error correction controller except by use of a physical device detecting a notch in a card. And, assuming one were attempting to reconstruct the Kobayashi reader into a single chip, Kobayashi contains no disclosure on how to incorporate a physical optical detector into a controller chip, let alone the controller-chip equivalent to a notch in the casing of a flash card.

Likewise, Kikuchi, the Petition's secondary reference, discloses no controller chip that has any of the claimed controller chip structures of US '549. Kikuchi discloses a controller chip that can be located either

on a reader[2] or on a flash card, A89:2-4, and that manages bad block mapping in firmware. A90:1-7. But Kikuchi has no disclosure of a controller chip that can interface to both flash cards that have controllers and those that do not have controllers, a requirement of the claims of US '549.

Neither reference alone nor both in combination discloses the controller chip claimed in US '549.

Further, HP's Petition did not argue to reconstruct the two references into a single controller chip having all the structures the controller chip claimed in US '549.

4. HP's References – Controllers and Compatibility

In its Petition, HP argued to combine Kikuchi's bad block mapping techniques into Kobayashi's ATA controller because both references disclosed "reader" ATA controllers that were the same as the ATA controller on the flash cards. A91:8-18. Critical to HP's argument that

[2] The Petition uses the term "adapter" for Kikuchi's reader – but since the claimed invention uses the term "adapter" for a structural part of the claimed controller chip, the terms are not equivalent for this analysis. We substitute the term reader for the Kikuchi adapter to avoid confusion.

it would be obvious to combine Kikuchi's bad block mapping techniques into Kobayashi's ATA controller was that both Kobayashi and Kikuchi disclosed ATA controllers that alternatively could be located on either a reader or a flash card. A91:13-18. Kobayashi disclosed that its ATA controller 124 was the same ATA controller 124 as appeared on flash cards. A88:6-13; A341:12:44-45. See also, A84, Figs. 14 and 15 from the Petition. The side-by-side figure illustrate two flash cards, one with ATA controller 124, Fig. 15, and one without, Fig. 14.

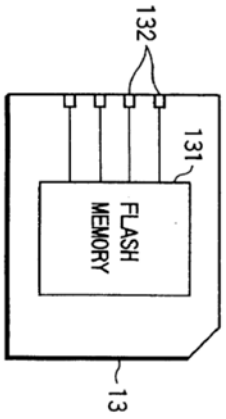

Figure 14: Flash Memory Card Without Controller (FIG. 2 of HP 1005)

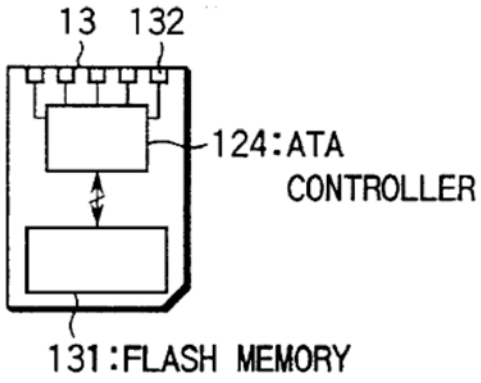

Figure 15: Flash Memory Card With Controller (124) (FIG. 10 of HP 1005)

Kikuchi provided a reader "ATA" controller 110 that, like the ATA controller 124 of Kobayashi, was functionally the same as the controller 10 on the flash card. A90:1-5, referencing Kikuchi Fig. 15A.

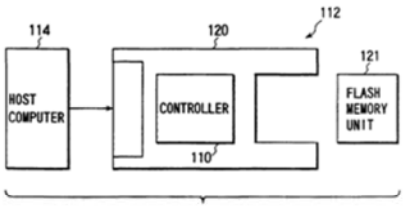

FIG. 15A

Figure 19: FIG. 15A of Kikuchi

Thus, similar to Kobayashi's ATA controller 124, Kikuchi discloses an ATA controller 10 that can be disposed in a flash memory card or in an adapter (controller 110) when the flash memory card has no controller. HP 1008 (Dr. Banerjee Decl.), ¶¶ 114-16.

Graphic from HP Petition at 49, A90

The references both disclosed that providing the same controller on the reader as that on the card assured compatibility between the ATA controller and the particular flash card. A342:13:9-10; A162:2-21.

Based on this, HP alleged that it would be obvious to combine Kikuchi's ATA controller bad block mapping techniques into Kobayashi's *ATA controller*. A90:8-11. Even if that were so, the resulting *ATA controller* of the Kobayashi *reader* does not disclose a controller chip as claimed in the '549 patent, and the combination relies on the fact that the ATA controller is the same on the reader as on the flash cards.

B. The Petition Is Barred Under 35 U.S.C. § 315(b)

The present IPR is barred by statute. Under 35 U.S.C. § 315(b), an IPR is barred if the petition requesting the proceeding is filed more than 1 year after the date on which petitioner, a real party in interest or a privy of petitioner is served with a complaint alleging infringement of the patent that is the subject of the petition. Such is the case here: a privy of Petitioner HP, Pandigital, Inc., was served with a complaint for infringement of US '549 more than a year before the filing of the Petition by HP. A1089, A1099-1100:p.47. MCM established that Pandigital, Inc. was a privy of HP at the time HP filed its Petition by virtue of their reseller relationship which made them successive owners of property with substantial substantive legal relationships. *Infra* at fns. 8 and 9. HP bought and resold Pandigital's accused digital picture frames ("DPF's"). *Ibid.* HP was notified of the US '549 infringement lawsuit against Pandigital, A1139, and of its own infringement of the '549 patent by virtue of selling DPF's. *Infra* at fn. 3. Moreover, while HP sells the accused DPF's under its own brand name, it identifies Pandigital as the manufacturer, and is reliant on Pandigital for

technical and warranty support of the DPFs for its customers. *Infra* at fns. 8 & 9.

In more detail, twice in 2008,[3] and once in 2010,[4] HP was notified of its infringement of US '549 by reason of its selling the Pandigital DPF's. (The accused DPFs have flash card readers with controller chips covered by the '549 patent). On September 21, 2011,[5] Pandigital was served with a complaint alleging infringement of US '549 by reason of its sale of DPFs[6] (the "Texas Action"). HP was notified of the Texas Action shortly after it was filed.[7] At the time of the Texas Action, and continuing through the filing of the IPR Petition on March 27, 2013, HP

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[3] A1142-7; A1148-54.

[4] A1155.

[5] A1117-A1118. (Notice of Appearance of James P. Martin on behalf of Pandigital)(The Sept. 21, 2011, service is at docket entry 24 of the Pandigital Action, see note 6.)

[6] A1089-A1116. *Technology Properties Limited LLC v. Pandigital, Inc.*, No. 2:11-cv-00372-TJW (E.D. Tex. 2011) (the "Texas Action"). The suit was stayed, A1166-7, pending the co-filed ITC proceeding: *Certain Digital Photo Frames and Image Display Devices and Components Thereof, Investigation,* No. 337-TA-807, instituted on Sept. 27, 2011, limited exclusion order against Pandigital, 78 Fed. Reg. 16707-9 (March 18, 2013)(The exclusion order excludes DPFs that infringe claims 1, 7, 11, 17, 19 and 21 of the '549 patent.) A1168-70.

[7] A1139-41. Notice was delivered to HP by both mail and e-mail to HP's president and various HP counsel.

resold Pandigital DPFs accused of infringement of US '549 under its own brand,[8] but identified Pandigital as their manufacturer, A1138, and referred customers seeking technical and warranty support to Pandigital.[9]

HP filed the present IPR on March 27, 2013, just nine days after the ITC issued a limited exclusion order against Pandigital ordering Pandigital to cease and desist from importing, offering for sale, distributing or soliciting the distribution of DPFs that infringe claims 7, 11, 19 and 21 of the '549 patent.[10]

C. The Board Relied on Federal Circuit Precedent To Sustain Constitutionality of The IPR Process

The Board relied on *Patlex Corp. v. Mossinghoff,* 758 F.2d 594 (Fed. Cir. 1985), to sustain the constitutionality of IPRs. The Board did

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[8] A1119-A1138 (User Guide); A1171-A1188 (Product Report: '549 claim chart vs. HP DF1010P1 digital picture frame); A1163-5 (Amazon.com); A1189-A1194 (Lum affidavit determining by reverse engineering that the DPFs HP were selling were the accused Pandigital DPFs.)

[9] A1160-A1162; A1161 (E-mail: customercare@pandigital.net).

[10] 78 Fed. Reg. 16707-9 (March 18, 2013)(The order excludes DPFs that infringe claims 1, 7, 11, 17, 19 and 21 of the '549 patent.) A1168-70, A1170, col. 1, ¶ 2.

not make an independent assessment of MCM's argument against the constitutionality of the IPR process. A4-5.

SUMMARY OF ARGUMENT

I. HP's Petition Did Not Allege Facts Sufficient To Support The Board's Decision of Invalidity

HP's Petition did not establish that Kobayashi disclosed a controller chip having 1) an interface mechanism as claimed, 2) a detector as claimed, and 3) a flash adapter as claimed. The Board's decision erroneously relies on HP's "assertion" that Kobayashi discloses every claim limitation of the challenged claims except bad block mapping error correction [Decision at p. 9, A9] when that "assertion" simply is not supported by the reference. The Board's reliance on the "assertion" without factual support from the reference is legal error: HP did not carry its statutory burden to prove unpatentability and the Board's reliance on HP's assertion (rather than on factual support) shifted the burden to MCM to refute facts not established in the Petition.

Nor did HP's Petition allege that Kikuchi disclosed the claimed controller chip. HP's Petition clearly used the Kikuchi reference to show management of bad block mapping in firmware. Combining these

two references does not ameliorate the fatal flaw that Kobayashi does not disclose the positively recited controller chip having the three positively recited structures claimed by US '549. Even when combined with Kikuchi, the resulting combination does not disclose all of the claim limitations of US '549. HP's Petition therefore did not establish – by a preponderance of the evidence or otherwise –that claims 7, 11, 19, and 21 are unpatentable. The IPR should not have resulted in a final decision of unpatentability. MCM is therefore entitled to a reversal.

II. HP's Petition Is Barred Under 35 U.S.C. § 315(b)

Under controlling law, *Taylor*[11] and *Aevoe*,[12] MCM demonstrated that Pandigital, Inc. was a privy of HP with respect to the very products that were subject to a complaint for patent infringement of the '549 patent, served on Pandigital more than a year prior to the filing of the IPR. By statute, the present IPR is barred under 35 U.S.C. § 315(b).

[11] *Taylor v. Sturgell*, 128 S. Ct. 2161, 2175, 2178 (2008).

[12] *Aevoe Corp. v. AE Tech Co., Ltd.*, 727 F.3d 1375, 1384 (Fed. Cir. 2013).

III. The IPR Proceedings Are Unconstitutional Under Controlling Authority Decided Since *Patlex*

An IPR is an action to revoke or cancel a patent that under *Marbury*, *McCormick Harvesting*, *Granfinanciera*, *Stern* and *Wood* must be tried in an Article III Court with access to a jury. *Patlex* has been overruled under *Troy v. Samson*, 758 F.3d 1322 (Fed. Cir. 2014).

ARGUMENT

I. Standard of Review

This court reviews legal conclusions of the Board *de novo* and factual findings for substantial evidence. *HIMPP v. Hear Wear Technologies, LLC.*, No. 2013-1549, Slip opinion at *5 (Fed. Cir. May 27, 2014):

> We review the Board's legal conclusions *de novo, In re Elsner,* 381 F.3d 1125, 1127 (Fed. Cir. 2004), and the Board's factual findings underlying those determinations for substantial evidence, *In re Gartside,* 203 F.3d 1305, 1316 (Fed. Cir. 2000). A finding is supported by substantial evidence if a reasonable mind might accept the evidence to support the finding. *Consol. Edison Co. v. NLRB,* 305 U.S. 197, 229 (1938). Obviousness is a question of law, based on underlying factual findings. *Graham v. John Deere Co.,* 383 U.S. 1, 17-18 (1966); *KSR Int'l Co. v. Teleflex Inc.,* 550 U.S. 398, 427 (2007). A claim is invalid for obviousness if, to one of ordinary skill in the pertinent art, "the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would

> have been obvious at the time the invention was made. . . ." 35 U.S.C. § 103(a) (2006); *see also KSR,* 550 U.S. at 406-07.

Ibid.

II. HP's Petition Did Not Contain References That Disclosed The Claimed Controller Chip

A. The Claims of US '549 Disclose a Controller Chip That Has Three Distinct Structures

The claims of US '549 at issue are all directed to a controller chip. Claim 11 defines the controller chip's structure. Claim 11 best illiterates the controller chip elements, the issues on appeal. Claim 11 requires the controller chip to have 1) **an interface mechanism**, 2) **a detector**, and 3) **a flash adapter**, each with specific further structural and/or functional requirements. Claim 7 identifies a method of using the controller chip with that structure. Claim 11 claims the structure. Claim 11:

> 11. A system comprising:
>
> a computing device;
>
> a flash storage system comprising a flash section and at least a portion of a medium ID; and
>
> a controller chip coupled between the computing device and the flash storage system to interface the flash storage system to the computing device,

> the controller chip comprising
>
> **an interface mechanism** capable of receiving flash storage systems with controller and controllerless flash storage systems,
>
> **a detector** to determine whether the flash storage system includes a controller for error correction and
>
> **a flash adapter** which comprises firmware to perform, in an event where the flash storage system does not have a controller for error correction, operations to manage error correction of the flash section, including bad block mapping of the flash section in the flash storage system that is coupled to the flash adapter section.

(Emphasis supplied.)

As claimed, the controller chip must, in addition to interfacing with flash storage systems (flash cards or simply cards) that have controllers and those that do not, must also be able to detect whether such a card has an error correction controller or not, and in the event that it does not have an error correction controller, manage bad block mapping (a form of error correction) in firmware.

B. Kobayashi Does Not Disclose The US '549 Limitations But For Bad Block Mapping

In its Petition, HP relied on Kobayashi's reader 12 to set forth all limitations of the claimed chip controller in US '549 but for bad block mapping. A9:2-3. Kobayashi, however, does not disclose any of the

limitations of US '549 directed to the controller chip. HP alleged that the only claim limitation missing from Kobayashi was the limitation directed to managing bad block mapping in firmware. *Ibid.* For example, for claim 11's controller chip limitation, the Petition states at A92-93, "Kobayashi describes a reader/writer 12, which includes a conversion controller 122, an ATA controller 124, and ROM 123 that interface flash memory cards 13 to computer 11." This is not a controller chip, but a reader.

For the "interface mechanism," the Petition cites Kobayashi Figs. 11 and 12 that disclose the entire reader, not an "interface mechanism" and certainly not "a controller chip comprising an interface mechanism…." A93.

As for the claimed detector, HP's Petition merely states that "Kobayashi discloses a sensor (133/133A/133B)," not a "controller chip comprising a detector to determine whether the flash storage system includes a controller for error correction." A93. In fact, Kobayashi *requires* a *mechanical optical reader* and a *physical differentiation in the flash card* in order to detect a difference in flash cards and not even necessarily a difference as to whether the flash card contains a

controller for error correction or not. A341:12:67-A342:13:2; A342:13:12-13. Moreover, neither reference relied upon by HP discloses how to put the function of the Kobayashi mechanical/optical sensor with its cooperating switch and card notch, into a controller chip, like the claimed controller chip.

Finally, HP states that, "Kobayashi discloses firmware to perform error correction for controllerless flash storage systems" A93, which is not the same as the US '549 limitation requiring "a controller chip comprising a flash adapter which comprises firmware to perform, in an event where the flash storage system does not have a controller for error correction, operations to manage error correction of the flash section, including bad block mapping of the flash section in the flash storage system that is coupled to the flash adapter section."

HP argues that the missing management of the bad block mapping in firmware "functionality" can be found in its second reference, Kikuchi. HP alleged that it would be obvious to combine this bad block mapping functionality into Kobayashi's *ATA controller 124*, one of the two controllers located on the Kobayashi reader 12. A93-A94. HP alleged this combination to be obvious, a work of one of ordinary

skill, a mere design choice, because, HP argued, Kikuchi's ATA controller (10, 110) could be alternatively located on a reader or on a flash card like Kobayashi's ATA controller 124. A91-A92.

The combination depends on the ATA controllers of both references being alternatively located on the reader or the flash cards, where, regardless of location, the ATA controller will work only with one type of flash card – those that do not have ATA controllers themselves. In contrast, US '549 is a reader-specific controller chip that detects whether a card has a "controller for error correction" and includes firmware in a flash adapter section of the controller chip that conducts operations to manage bad block mapping of the flash section of the flash card in the event that the flash card does not have a controller for error correction.

The Board, provides no support for a factual finding that Kobayashi discloses the challenged claims of US '549 in its Decision and cites only to HP's "assertion" that Kobayashi makes those disclosures. A9. Other than HP's "assertion," the factual record does not substantiate the Board's finding. Therefore, the finding is not supported by substantial evidence and must be reversed.

C. Kobayashi and Kikuchi – Single Controller Chip

In its Petition, HP did not argue that Kikuchi disclosed a single controller chip that contained Kobayashi's functionality. Nor did HP argue to reconstruct Kobayashi into one controller chip based on any Kikuchi teaching. The Board's Decision acknowledges that the Petition never "explicitly" argued the "single chip requirement" with respect to Kobayashi. A9:24-26. Instead the Board relied on Kikuchi for disclosing the "single-chip limitation" because Kikuchi disclosed a single controller chip. A10:4-10.[13] But the challenged claims of US '549 require a controller chip having three distinct structures – yet HP never made any argument that Kobayashi was missing any limitation but the bad block mapping limitation. HP's Petition referenced Kikuchi only to establish that it disclosed bad block mapping in firmware in an ATA controller chip that could alternatively be located on a reader and a flash card, and in no fashion made any argument that Kikuchi could be

[13] The Board's Decision never mentioned and therefore did not seem to understand HP's argument that both references required that the ATA controllers of both references be alternatively located on readers and flash cards.

used to argue that Kobayashi be reconstructed into a single controller chip.

HP's argument to combine Kikuchi into Kobayashi for the missing bad block mapping functionality requires that the Kikuchi controller chip be the same controller chip regardless of whether it is located on a flash card or on a reader. HP's Petition argued that it would be obvious to combine Kikuchi's bad block mapping techniques into Kobayashi's ATA controller because Kikuchi's controller chip could be alternatively located on the flash card or on the reader just like Kobayashi's ATA controller. The Board entirely missed that combining the references does not, in fact *cannot*, yield a single controller chip because Kobayashi requires the controller be the same on the reader and the card. Indeed, HP did not make the argument the Board constructed regarding a single controller chip because to do so would be antithetical to the Kobayashi reference.

The Board's findings regarding Kikuchi's controller chip disclosure and HP's arguments with respect thereto are contrary to the record and therefore its Decision must be reversed.

D. HP's Obviousness Argument

The Board's Decision *ignores* the only obviousness argument HP did in fact make in its Petition, and which was critical to its case: that both references disclosed ATA controllers (Kobayashi's 124 and Kikuchi's 10) that work "regardless of location," whether located on a card or located on a reader (because they were functionally the same). A91. The Board's decision stated instead that HP had argued that both references "describe ATA controllers that work with flash-memory cards with, or without, on-card controllers." A9. This finding is contrary to the evidence. HP never made that argument or provided evidence to substantiate that statement. Both references disclose ATA controllers that can be located on either a reader or on a flash card because the controllers are the same "controller chip." But neither reference discloses an ATA controller or chip that works *with* flash cards that have their own ATA controllers. In both references, the ATA controllers located on a reader work only *with flash cards that do not have their own ATA controller*.

What HP in fact argued was this:

> It would have been obvious to one of ordinary skill in the art at the time of the effective filing date of the '549 Patent to

> incorporate Kikuchi's error correction and ATA controller bad block mapping techniques into ATA controller 124 of Kobayashi "to reliably retain stored data." … Because both Kobayashi and Kikuchi describe ATA controller functionality as the same regardless of the controller's location in a flash memory card or in an external adapter, the modified ATA controller 124 in reader/writer 12 of FIGS. 11 and 12 of Kobayashi would perform error correction and bad block mapping as expressly taught by Kikuchi in the event the inserted flash memory card does not have a controller built therein."

A91.

To the same effect, the Board misstated the Petition's discussion of HP's KSR arguments. The Decision states that the Petition argued "that combining the teachings of the two references is merely 'the combination of prior art elements according to known methods to yield predictable results' (PET. 50-51)." A10. However, the Petition actually argued,

> For at least the foregoing reasons, combining the ECC and bad block mapping teachings of Kikuchi with the teachings of Kobayashi is merely: (a) a combination of prior elements according to known methods to yield predictable results…

A91-A92. The arguments made by the Petition are specific to the ECC and bad block mapping teachings. The Board's restatement implies that HP argued somehow to reconstruct Kobayashi into one chip. That notion is not supported by HP's actual argument.

But most importantly, the Decision left the impression that both Kikuchi and Kobayashi disclosed ATA controllers that could work *with* flash cards that had controllers or alternatively *with* flash cards that had no controllers when in fact neither have this capability.

E. Kobayashi's Physical/Optical Detector Is Not a Circuit

Even if HP had argued to reconstruct Kobayashi into one chip, Kobayashi cannot be reconstructed into one chip because its physical/optical detector is a physical structure, not a circuit. If one were to reconstruct Kobayashi to provide a controller chip having all the functionality of the various controllers of Kobayashi's Fig. 11 (122, 123, 124) and selector switch 134, *supra*, that controller chip still would not contain any functionality or structures of the physical mechanical optical/detector 133, which HP alleged corresponded to the *claimed* detector in US '549, and which is a controller chip structure that must be present in a prior art controller chip to anticipate or render obvious the claimed controller chip because the claimed controller chip requires the detector be a structure of the controller chip. Neither Kobayashi nor Kikuchi disclose any method or means by which a controller chip might determine whether a flash card has a controller for error

correction or not other than by means of a physical/optical detector that clearly is not part of any controller chip and which cannot be made part of any controller chip because it is not a circuit, but a physical structure. HP's Petition simply ignored the requirement that the detector be part of the claimed controller chip. The Board failed to recognize this critical distinction despite MCM repeatedly arguing that HP's petition ignored the requirements of the claimed controller chip and despite MCM arguing during oral argument that one of ordinary skill could not put a physical optical detector into a controller chip. A254:23-A255:3; A259:2-6.

F. Hypothetical Kobayashi

Moreover, even if Kobayashi could be reconstructed into one controller chip, that chip would not be the same as the chip on the flash card. Any hypothetical reconstructed controller chip that had all the structures and functions required of it by the claims would then not be the *same* controller chip as the ATA controller chip located on the flash card as Kobayashi discloses as being required for its reader to operate. HP argued that this was *the reason* that one would find it obvious to combine Kikuchi's bad block mapping techniques into Kobayashi's ATA

controller because both references disclose ATA controllers that could alternatively be located on a reader and on a flash card because *they were the same controller*. A88:6-13; A89:2-5; A91:12-18.

G. The Board's Obviousness Argument

HP did not argue the obviousness argument relied upon by the Board. The reasoning stated in the Board's Decision clearly shows that the Board erroneously shifted the burden to MCM to rebut an obviousness argument that the Petition neither made nor was supported with facts.

> Patent Owner does not argue that applying the teachings of Kikuchi and Kobayashi so that the claimed functionality is on a single chip would have been "uniquely challenging or difficult for one of ordinary skill in the art"…

A10.

MCM did not argue this point in its Patent Owner Response because it is *not* in response to *anything that the HP Petition argued*. At no point in HP's Petition was the argument ever made, in any form, that Kobayashi should be reconstructed into a single chip or that Kikuchi discloses a controller chip having any of the claimed functionality or structures of US '549, let alone all of them. Had HP made these arguments it would have been blatantly inconsistent with

the obviousness argument HP did make: that the reason for combining Kobayashi and Kikuchi in the first instance was that their ATA controllers were functionally the same as the controllers on the flash cards so that when located on the reader, they would work the same as when they were located on the flash card. It is clear in the Board's Decision that it did not appreciate the role of the ATA controller, particularly in Kobayashi and how it was critical in HP's obviousness argument. Had the Board recognized that the ATA controller had to be the same controller on both the reader and on the flash cards, the Board would have realized why HP never argued to reconstruct Kobayashi into one chip, and why reconstructing Kobayashi into one chip was not simply a design choice.

Controlling law requires a proponent to argue where the references disclose or render obvious the claim limitations at issue, here the claimed controller chip having all the claimed structures and functions. *Fleming v. Escort*, No. 14-1331, *6 (Fed. Cir. Dec. 24, 2014), citing to *Koito Mfg. Co. v. Turn-Key-Tech, LLC*, 381 F.3d 1142, 1152 (Fed. Cir. 2004), which in turn cited to *Schumer v. Lab Computer*

Systems, Inc., 308 F.3d 1304, 1315-16 (Fed. Cir. 2002) for the proposition that

> [T]estimony concerning anticipation must be testimony from one skilled in the art and must identify each claim element, state the witnesses' interpretation of the claim element, and explain in detail how each claim element is disclosed in the prior art reference. The testimony is insufficient if it is merely conclusory.

Koito Mfg., *supra*, at 1152. HP did not argue that Kobayashi be reconstructed into one chip: in fact it could not argue that it be reconstructed into one chip without denying the very essence of Kobayashi. The Board's basing their unpatentability Decision on an argument that Petitioner HP did not make is reversible error. Likewise, putting the burden on MCM to rebut an argument that the Petition did not make is reversible error. Moreover, basing its finding of unpatentability on a fictional combination of references that do not comport to the references themselves is reversible error.

The Board raised the question of reconstructing Kobayashi in oral argument even though HP's Petition never made such an argument. There, MCM *did* argue that it was *beyond the skill in the art* to put a physical optical detector into a chip, the structures Kobayashi provides for the claimed detector limitation. A portion of the following, lines 5-

12, was quoted in the Decision. The argument that the Board states in its Decision MCM did not make is in **bold** below.

JUDGE BISK: Is there some reason not to put them on a single chip? It seems like it is just a design choice, whether it is one chip, two chips, 10 chips.

Is there a particular reason why the number of chips matters?

MR. HELLER: It is not that. It is, why would you do that? Why would you put all that functionality into a single chip?

Let's go back to the figure for one second and take a look at what Kobayashi actually discloses.

It discloses the use of an ATA controller 124. That is the same controller that is on the flash cards.

Now, if you put that ATA controller into a single chip, that ATA controller cannot be the same controller on the flash cards. It would defeat the whole purpose of Kobayashi to put the same controllers on the flash cards into the reader.

I mean, you basically are defying, defying Kobayashi to do the reconstruction according to our claimed invention.

Now, once you decide to put the functionality of two circuits together into one larger integrated circuit, it is well within the skill of the art. **Perhaps you could figure out how to put an optical, a physical optical detector into a chip, but I think you can't do that, but our claims require that functionality, and we disclose how to do it in our specification**.

We have this medium ID, and that is in the claims. All that functionality is not in Kobayashi. And there is no suggestion by Hewlett-Packard in its petition to combine -- reconstruct Kobayashi according to our claims.

They just proved that Kobayashi somewhere scattered about on this reader has the functionality of our claimed invention.

Record of Oral Hearing, Doc. No. 30, A228 at A258-9. MCM argued that reconstructing Kobayashi as suggested by the Board would "defeat the whole purpose of Kobayashi to put the same controllers on the flash cards into the reader." Thus, reconstructing Kobayashi was not merely a design choice as suggested by Judge Bisk. To do so would undo, "defy" Kobayashi and use hindsight to reconstruct Kobayashi "according to our claimed invention." A258:17-24.

H. MCM Must Prevail on This Record

> 35 USC 316(e) EVIDENTIARY STANDARDS.—In an *inter partes* review instituted under this chapter, the petitioner shall have the burden of proving a proposition of unpatentability by a preponderance of the evidence.

HP is statutorily not entitled to prevail because 35 U.S.C. § 316(e) places a mandatory, statutory burden of proof ("shall have the burden") on HP, and the only evidence HP provided is its Petition. Controlling case law authority requires that HP prove that all limitations are disclosed in the prior art. *PAR Pharmaceuticals v. TBI Pharmaceuticals*, 14-1391, *12-17 (Fed. Cir. 2014). Just as in *PAR Pharmaceuticals,* the Petition "ignores the claim limitations at issue." *Id.* at *16. In its Petition, HP does not produce any evidence that establishes that all the limitations of the challenged claims are

disclosed in the prior art. HP's prior art references do not disclose a controller chip having *any* of the claimed functionality or structures, let alone all of them. Nor does HP's Petition contain any argument that Kobayashi be reconstructed into a single controller chip, which is foundational to the Board's Decision. It is manifest that even after being modified by Kikuchi in a manner argued by the Petition (to modify Kobayashi's ATA controller to implement Kikuchi's bad block mapping) that Kobayashi discloses no controller chip that

- interfaces with cards that have controllers and cards that do not;
- has a detector for determining whether a card has a controller for error correction; or
- manages bad block mapping of the flash card in the event that a flash card does not have a controller for error correction.

On this record, reversal of the Board's Decision is required.

III. This IPR Is Barred Under 35 U.S.C. § 315(b)

A. Section 315(b) Limits The Board's Authority To Institute An *Inter Partes* Review

35 U.S.C. § 315(b) states:

> (b) PATENT OWNER'S ACTION.—An inter partes review may not be instituted if the petition requesting the proceeding is filed more than 1 year after the date on which

> the petitioner, real party in interest, or privy of the petitioner is served with a complaint alleging infringement of the patent.

The Board's authority is not discretionary under § 315(b): that is, if a privy of Petitioner is served with a complaint alleging infringement of the patent more than a year prior to the filing of the Petition, then the Petition is barred and the Board has no authority to undertake a review.

B. The Burden Is On The Petitioner To Demonstrate Standing

Section 312 specifies the mandatory requirements for the petition. Section 312(a)(4) provides that "the petition provides its other information as the Director may require by regulation." Rule 42.104(a) specifies that the petition must set forth that the "petitioner is not barred or estopped from requesting an inter partes review…." Rule 41.8(a)(2) (mandatory notices) requires a party to a contested case to identify "[e]ach judicial or administrative proceeding that could affect, or be affected by, the Board proceeding."

HP's Petition failed to identify the Texas Action in its mandatory notices even though HP had notice of the Texas Action. A42. HP's Petition failed to state that HP was a reseller of Pandigital DPFs, which

were the subject of an Exclusion Order just nine days prior to the filing of its Petition. A1139. HP likewise did not disclose the nature and extent of its relationship with Pandigital as established in the evidence submitted by MCM. At a minimum, HP had sufficient facts to put it on a duty of inquiry concerning its relationship to Pandigital because, on at least three different occasions, HP had been previously notified of its infringement of US '549 by virtue of its selling of DPFs. A1142-7; A1148-54; A1155. Despite this, HP made the certification required by Rule 42.104(a) without disclosure of any of these facts.

The burden of proving standing remains on HP, yet HP presented no evidence or argument in rebuttal to MCM's evidence and argument made in its Preliminary Response. The facts MCM presented therefore are undisputed and admitted. Because HP is reselling accused Pandigital DPFs the fact that HP and Pandigital are privies with respect to DPFs accused of infringing US '549 is undisputed. *Cf.*, *Aevoe Corp. v. AE Tech Co., Ltd.*, 727 F.3d 1375, 1384 (Fed. Cir. 2013)(A reseller of accused products is in privity with a party-defendant such that they might be bound by a preliminary injunction of which they had notice). It is also undisputed that Pandigital was served with a

complaint for patent infringement of the '549 patent outside the one year limit imposed by § 315(b). *Supra* at note 6. Under the undisputed facts Pandigital is an admitted privy of HP, and therefore § 315(b) bars the present IPR.

Despite that the facts and that the relationship of privity between HP and Pandigital were undisputed, the Board decided that MCM had not proven HP-Pandigital privity for § 315(b) *purposes* because MCM provided "no persuasive evidence that HP could have exercised control over Pandigital's participation in the Texas Action." A20.

MCM moved for rehearing based on this court's opinion in *Aevoe*, a case that was decided after MCM had filed its preliminary response. A136. The Board denied rehearing on October 13, 2013, A31, stating that "the allegedly infringing articles referred to by MCM are *not at issue in this proceeding*." A33 (emphasis added). It is unclear what the Board intended this to mean. It is undisputed, however, that the Petition is for an IPR of US '549 and it is undisputed that the facts establish a relationship of privity between HP and Pandigital with respect to products accused of infringing US '549 (the Pandigital DPFs that HP resold).

C. The Board's Denial Of Privity For The Purposes Of § 315(b) Is Erroneous

On October 23, 2013, MCM petitioned this court for a writ of mandamus with respect to the § 315(b) bar. On February 18, 2014, this court denied the petition without prejudice. *In re MCM Portfolio, LLC*, No. 14-104 (Fed. Cir. 2014). In doing so, this court noted that a

> "Privy" generally refers to a "sufficiently close relationship" between the purported privy and the relevant other party such that both should be bound by the trial outcome and related estoppel provisions. *Office Patent Trial Guide*, 77 Fed. Reg. 48759 (Aug. 14, 2012); see also generally *Int'l Nutrition v. Horphag Research*, 220 F.3d 1325, 1329 (Fed. Cir. 2000) ("A variety of relationships between two parties can give rise to the conclusion that a nonparty to an action is 'in privity' with a party to the action for purposes of the law of judgments, which is simply a shorthand way of saying that the nonparty will be bound by the judgment in that action.").

Id. at *2. It must be noted that *Int'l Nutrition* continued,

> One situation in which parties have frequently been held to be in privity is when they hold successive interests in the same property. *See, e.g., Litchfield v. Crane,* 123 U.S. 549, 551, 8 S.Ct. 210, 31 L.Ed. 199 (1887) (defining privity to include a "mutual or successive relationship to the same rights of property").

Id. at 1329. Thus *Int'l Nuitriton* directly supports MCM's privity position.

Under controlling Federal Circuit law, therefore, including both *Aevoe* and *Int'l Nutrition*, and as admitted by HP, HP is in legal privity with Pandigital with respect to the DPFs accused of infringement of US '549 in the Texas Action because HP is a reseller of the very same products accused of infringement of US '549.

The source of the Board's error lies in the *Office Patent Trial Practice Guide's*[14] misreading of *Taylor v. Sturgell,* 553 U.S. 880 (2008) to authorize a balancing of its six distinct categories[15] of privity in an equitable stew of "factors" akin to the various flavors of "virtual representation."[16] However, the Supreme Court categorically overruled

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[14] *Office Patent Trial Practice Guide*, 77 Fed. Reg. 48756 (Aug. 14, 2012).

[15] The six categories are 1) the nonparty agrees to be bound; 2) "preexisting" legal relationships including preceding and succeeding owners of property; 3) the nonparty is adequately represented by someone with the same interests; 4) nonparty assume control over the litigation; 5) the nonparty is litigating through a proxy; and 6) a special statutory scheme may foreclose further litigation. *Taylor,* 553 U.S. at 893-895.

[16] *Id.* at 888-890. The Court cited the D.C. Circuit that the Circuits varied widely in their approach to virtual representation, all of which specified a variety of factors that were weighed, and proceeded to adopt its own five-factor test. *Ibid.*

virtual representation, *id.* at 904, and flatly rejected any "flavor of equitable balancing":

> Fairchild and the FAA do not argue that the D.C. Circuit's virtual representation doctrine fits within any of the recognized grounds for nonparty preclusion. Rather, they ask us to abandon the attempt to delineate discrete grounds and clear rules altogether. Preclusion is in order, they contend, whenever "the relationship between a party and a non-party is 'close enough' to bring the second litigant within the judgment." Brief for Respondent Fairchild 20. See also Brief for Respondent FAA 22-24. Courts should make the "close enough" determination, they urge, through a "heavily fact-driven" and "equitable" inquiry.
> …
>
> We reject this argument….

Id. at 898.

In *Taylor*, the Supreme Court explicitly rejected an equitable balancing test in favor of the six specified categories set forth therein. By giving "controlling" weight to *Taylor* category 4 (i.e., control over the litigation), the Board elected a different test for privity than established by the Supreme Court. *Taylor* category 4 relates to "control" by the nonparty petitioner of the party served with a complaint for patent infringement. By requiring a demonstration of control, the Board ignored controlling Federal Circuit and Supreme Court precedent on privity under *Taylor*, *Aevoe* and *Int'l Nutrition* pursuant to which MCM

established that Pandigital was HP's privy. Instead, the Board found control over litigation determination, effectively deciding that successive-owners-of-property privity, as set forth in *Taylor* category 2, is not by itself sufficient "for § 315(b) purposes."

The undisputed facts establish the relationship of privity between HP and Pandigital and therefore MCM is entitled to a reversal of the Board's decision regarding § 315(b). The decision to institute the IPR was barred by § 315(b) and must be vacated.

IV. Actions To Revoke Or Cancel A Patent Must Be Adjudicated In An Article III Court With Access To A Jury In Accordance With The Seventh Amendment Of The Constitution

A. Actions To Revoke Or Cancel A Patent Must Be Tried In Article III Courts

It is well-established that a patent is constitutionally protected property and "is as much entitled to protection as any other property." *Cammeyer v. Newton*, 94 U.S. (4 Otto) 225, 234-35 (1876); *see also James v. Campbell*, 104 U.S. 356, 357-58 (1881); *Crozier v. Fried, Krupp Aktiengesellschaft*, 224 U.S. 290, 306 (1912). The Supreme Court held

in *Marbury v. Madison* that the question whether a property right may be revoked lies within the exclusive province of the Courts.[17]

Accordingly, the Supreme Court held in *McCormick Harvesting Machine Co. v. Aultman*, 169 U.S. 606, 18 S. Ct. 443, 42 L. Ed. 875 (1898) that the Commissioner of Patents had no constitutional power to revoke or to cancel a patent, that being the exclusive province of the Courts, and wrote:

> It has been settled by repeated decisions of this court that when a patent has received the signature of the Secretary of the Interior, countersigned by the Commissioner of Patents, and has had affixed to it the seal of the Patent Office, it has passed beyond the control and jurisdiction of that office, and is not subject to be revoked or cancelled by the President, or any other officer of the Government. … It has become the property of the patentee, and as such is entitled to the same legal protection as other property.
>
> …
>
> The only authority competent to set a patent aside, or to annul it, or to correct it for any reason whatever, is vested in the courts of the United States, and not in the department which issued the patent.

Id. at 608-609.[18]

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[17] *Marbury v. Madison*, 5 U.S. 137, 154-56, 166 (1803).

[18] *McCormick* cites *U.S. v. Schurz*, 102 U.S. 379 (1890) which traces the doctrine to *Marbury*. *Id.* at 395.

B. The *Patlex* Reasoning Is Inconsistent With *Mccormick Harvesting*

This Court, in *Patlex Corp. v. Mossinghoff*, 758 F.2d 594, 604 (Fed. Cir. 1985), upheld the constitutionality of the Commissioner's statutory power[19] to administratively revoke or cancel a patent. *Patlex* held that a patent was a public right, "a right that can only be conferred by the government," citing *Crowell v. Benson*, 285 U.S. 22 (1932), and thereby sought to distinguish the private rights involved in *Northern Pipeline Constr. Co. v. Marathon Pipe Line Co.*, 458 U.S. 50 (1982), as limited to "common law disputes historically adjudicated by Article III courts." *Id.* at 604. The *Patlex* court also reasoned that *McCormick* could be distinguished because the procedure involved there was a Reissue to correct mistakes made by the patent owner, whereas the procedure involved in *Patlex* was a Reexamination to correct mistakes made by the government.

> The holding of *McCormick Harvesting* may also be distinguished, in view of Congressional intent to provide a separate procedure for reexamination while preserving the reissue practice. The purpose of reissuance of patents is to enable correction of errors made by the inventor, at the

[19] Pub.L. No. 96-517 § 1, 94 Stat. 3015 (1980), effective date July 1, 1981, codified as 35 U.S.C. §§ 301-307.

> initiative of the inventor. The reexamination statute's purpose is to correct errors made by the government, to remedy defective governmental (not private) action, and if need be to remove patents that should never have been granted. We do not read *McCormick Harvesting* as forbidding Congress to authorize reexamination to correct governmental mistakes, even against the will of the patent owner.

Id. at 604.

However, the *Patlex* reasoning is inconsistent with *McCormick* and its predecessor cases that consistently held that once the patent has issued, it is the property of the patent owner and cannot be revoked by the Government for mistake, and that if there is a governmental mistake, the government has a judicial remedy only if it has a direct interest in the matter:

> In the case of a patent for lands it has been held that when one has obtained a patent from the Government he cannot be called upon to answer in regard to that patent before the officers of the Land Department, and that the only way his title can be impeached is by suit. ... But a suit may be maintained by the United States to set aside a patent for lands improperly issued by reason of mistake, or fraud; but only in the case where the Government has a direct interest, or is under obligation respecting the relief invoked.

Id. at 609.

The object of *Marbury* and of *McCormick Harvesting* is to prevent the government from unilaterally revoking or repealing an issued

patent for *any* reason. Patents are the property of their owners and even the government must resort to the Courts if there is a mistake, regardless of who made the mistake. In short, *Patlex* was incorrect when it was decided, because it was inconsistent with governing Supreme Court precedent.

C. The *Patlex* Decision Is Inconsistent With Subsequent Supreme Court Cases On The "Public Rights" Doctrine

Moreover, *Patlex* should be overruled because it is inconsistent with two separate lines of subsequent Supreme Court decisions. First, *Patlex*'s view of the "public rights" doctrine was rejected in *Stern v. Marshall*, 131 S.Ct. 2594, 564 U.S. 2 (2011), where the Court held that a bankruptcy court's judgment of a bankruptcy estate's permissive state-law counterclaim against a creditor who had filed a claim against the estate violated Article III. The Court rejected the argument that the counterclaim could be classified as a "public right," explaining that the public rights doctrine extends only to cases where the government was acting in its *sovereign capacity* with respect to persons subject to its authority in connection with the performance of the constitutional functions of the executive or legislative departments" (emphasis

supplied). More specifically, that the exception does not extend to "property cases", writing at pages 2612-3:

> "Subsequent decisions from this Court contrasted cases within the reach of the public rights exception—those arising "between the Government and persons subject to its authority in connection with the performance of the constitutional functions of the executive or legislative departments"—and those that were instead matters "of private right, that is, of the liability of one individual to another under the law as defined." *Crowell v. Benson,* 285 U.S. 22, 50, 51, 52 S.Ct. 285, 76 L.Ed. 598 (1932).[6] See *Atlas Roofing Co. v. Occupational Safety and Health Review Comm'n,* 2613*2613 430 U.S. 442, 458, 97 S.Ct. 1261, 51 L.Ed.2d 464 (1977) (Exception extends to cases "where the Government is involved in its sovereign capacity under ... [a] statute creating enforceable public rights," while "[w]holly private tort, contract, and property cases, as well as a vast range of other cases ... are not at all implicated"); *Ex parte Bakelite Corp.,* 279 U.S. 438, 451-452, 49 S.Ct. 411, 73 L.Ed. 789 (1929). See also *Northern Pipeline, supra,* at 68, 102 S.Ct. 2858 (plurality opinion) (citing *Ex parte Bakelite Corp.* for the proposition that the doctrine extended "only to matters that historically could have been determined exclusively by" the Executive and Legislative Branches)"

Id., 131 S.Ct. 2594, at 2612-3.

Stern's understanding of the "public rights" doctrine is correct. The term was coined in *Murray's Lessee v. Hoboken Land & Improvement Co.*, 59 U.S. 272 (1856), where a NYC customs collector had withheld $1.3 million in collected duties, and a treasury officer issued a warrant for the sale of his property to recoup the withheld

duties. The Supreme Court noted that the English government traditionally dealt with its tax collectors as a matter of sovereign right without using the Court system. Thus, the Supreme Court coined the term "public right" to denote the government acting in its sovereign capacity in areas traditionally reserved for the executive, writing that:

> To avoid misconstruction upon so grave a subject, we think it proper to state that we do not consider congress can either withdraw from judicial cognizance any matter which, from its nature, is the subject of a suit at the common law, or in equity, or admiralty; nor, on the other hand, can it bring under the judicial power a matter which, from its nature, is not a subject for judicial determination. At the same time there are matters, involving public rights, which may be presented in such form that the judicial power is capable of acting on them, and which are susceptible of judicial determination, but which congress may or may not bring within the cognizance of the courts of the United States, as it may deem proper. Equitable claims to land by the inhabitants of ceded territories form a striking instance of such a class of cases; and as it depends upon the will of congress whether a remedy in the courts shall be allowed at all, in such cases, they may regulate it and prescribe such rules of determination as they may think just and needful. Thus it has been repeatedly decided in this class of cases, that upon their trial the acts of executive officers, done under the authority of congress, were conclusive, either upon particular facts involved in the inquiry or upon the whole title.
>
> …
>
> To apply these principles to the case before us, we say that, though a suit may be brought against the marshal for

> seizing property under such a warrant of distress, and he may be put to show his justification; yet the action of the executive power in issuing the warrant, pursuant to the act of 1820, passed under the powers to collect and disburse the revenue granted by the constitution, is conclusive evidence of the facts recited in it, and of the authority to make the levy…

Id. at 284-285.

An IPR proceeding does not involve the government acting in its sovereign capacity in connection with the performance of the constitutional functions of the executive such as tax collection. In creating the IPR, Congress was not authorizing an activity which the executive has traditionally performed in its sovereign capacity. Instead, Congress authorized the transfer of patent validity adjudications from Article III Courts to the USPTO, thereby denying Patent Owners access to a jury trial in violation of the Seventh Amendment.

Patlex is inconsistent with a second line of subsequent Supreme Court cases. In *Granfinanciera, SA v. Nordberg*, 492 U.S. 33, 53-55 (1989), the Supreme Court held that a right which had been adjudicated in either the Law Court, the Equity Court, or the Admiralty Court in England prior to 1791 was not a public right, and that if such an adjudication was in the Law Court, the adjudication was subject to a

jury trial. Accordingly, patents cannot be public rights under *Granfinanciera* for at least two reasons. First, because infringement actions must be subject to adjudication by a jury. *Markman v. Westview Instruments, Inc.*, 517 U.S. 370, 377 (1996):

> Equally familiar is the descent of today's patent infringement action from the infringement actions tried at law in the 18th century, and there is no dispute that infringement cases today must be tried to a jury, as their predecessors were more than two centuries ago.

And, second, because actions to revoke or cancel a patent were in the nature of a writ *scire facias*[20] under which disputed facts had to be subject to a trial by jury. *Ex parte Wood & Brundage*, 22 U.S. 603 (1824) where the Court ordered a trial by jury in an action to revoke or repeal a patent because it was in the nature of a writ *scire facias*:

> … It is ORDERED by the Court, that a peremptory mandamus issue … that the said Judge do award a process, in the nature of a *scire facias,* to the patentees, to show cause why the said patent should not be repealed, … and that if the issue be an issue of fact, the trial thereof be by a jury …

Id. at 615.

[20] The writ *scire facias* is abolished at Fed. R. Civ. P. 81(b).

The writ *scire facias* to repeal a patent was filed in the common law side of Chancery[21] and was subject to adjudication by a jury with respect to disputed facts.[22] The writ is extensively discussed in Lemley, Mark A. "Why Do Juries Decide If Patents Are Valid?" *Va. L. Rev.* 98 (2013): 1673-1893, particularly in Part I, where the author concludes:

> The history I discuss in Part I blows up the myth that patent issues were tried to juries only if damages were at issue. Both equitable infringement suits in Chancery and *scire facias* actions were referred to juries to resolve fact disputes, despite the fact that neither involved claims for damages.

Id. at 1733.

---

[21] John Paxton Norman, *The Law and Practice Relating to Letters Patent for Inventions* (London: Butterworths, 1853) at 194 (Google Books); Holdsworth, William Searle. *A history of English law*. Vol. 1. Methuen, 1922, at 452 (Google Book).

[22] J. P. Norman, *supra* at n.15, at 203: "The Chancellor, though a common law judge, has no power to summon a jury. Therefore, if there are issues in fact, the Court of Chancery cannot try the issues, but the Lord Chancellor delivers the record by his proper hands into the common law Court ... to be tried there." *See also*, Chesnin, Harold, and Geoffrey C. Hazard Jr. "Chancery Procedure and the Seventh Amendment: Jury Trial of Issues in Equity Cases Before 1791." *Yale LJ* 83 (1973): 999 (PDF) where the author demonstrates that prior to 1800, all issues of fact arising in Chancery were tried to juries at Kings Bench.

D. *Patlex* Has Been Overruled By *Granfinanciera* (1989), *Markman* (1998) And *Stern v. Marshal* (2011) Based On *Wood* (1824)

In *Troy v. Samson*, 758 F.3d 1322 (Fed. Cir. 2014), this Court held that its decisions are effectively overruled by subsequent Supreme Court holdings that are "inconsistent" in their theory or reasoning with this Court's prior decisions, writing that:

> "[T]he issues decided by the higher Court need not be identical to be controlling. Rather, the relevant Court of last resort must have undercut the theory or reasoning underlying the prior circuit precedent in such a way that the cases are clearly irreconcilable." … Indeed, lower Courts are "bound not only by the holdings of higher Courts' decisions but also by their 'mode of analysis.'"

Id. at 1326. (Cited authority omitted.)

Such is the case with *Patlex*. *Patlex* has been overruled by *Granfanciera* (1989), *Markman* (1998) and *Stern v. Marshall* (2011). *McCormick Harvesting* and *Wood* remain good law standing for the proposition that actions to revoke or cancel a patent must be subject to adjudication by a jury in an Article III Court.

CONCLUSION AND RELIEF SOUGHT

- Reversal of the Final Written Decision that claims 7, 11, 19 and 21 are unpatentable.
- Reversal of the Board's Decision on § 315(b) and an order vacating the Institution Decision.
- An order vacating the Institution Decision as a violation of MCM's constitutional rights to have the validity of its patent determined in an Article III Court with access to a jury.

Respectfully submitted,

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Dated: January 20, 2015

ADDENDUM

ADDENDUM A

PTAB Document No.	Date	Document Description	Pages Included	Pages
31	08/06/2014	Final Written Decision	All	A1-A13
10	09/10/2013	Decision Institution of Inter Partes Review	All	A14-A30
19	10/10/2013	PTAB Decision – MCM Request for Rehearing	All	A31-A34
20	10/10/2013	Errata to Decision to Institute	All	A35-A36
1001	10/23/2013	US Patent No. 7,162,549	All	A271-A324

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Paper 31
Entered: August 6, 2014

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

HEWLETT-PACKARD COMPANY,
Petitioner,

v.

MCM PORTFOLIO, LLC,
Patent Owner.

Case IPR2013-00217
Patent 7,162,549

Before JONI Y. CHANG, GLENN J. PERRY, and JENNIFER S. BISK, *Administrative Patent Judges.*

BISK, *Administrative Patent Judge*.

FINAL WRITTEN DECISION

35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

A. Background

Petitioner Hewlett-Packard Company ("HP") filed a Petition (Paper 2, "Pet.") to institute an *inter partes* review of claims 7, 11, 19, and 21 (the "challenged claims") of U.S. Patent No. 7,162,549 (Exhibit 1001, "the '549 patent") under 35 U.S.C. §§ 311-319. Patent Owner MCM Portfolio, LLC ("MCM") filed a Preliminary Response. Paper 9. On September 10, 2013, we instituted trial (Paper 10; "Decision"), concluding that Petitioner had demonstrated a reasonable likelihood of showing that the challenged claims are unpatentable under 35 U.S.C. § 103 over U.S. Patent No. 6,199,122 (Ex. 1005) ("Kobayashi") combined with WO 98/03915 (Ex. 1007) ("Kikuchi"). Decision 3, 16.

We have jurisdiction under 35 U.S.C. § 6(c). This final written decision is issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73.

Petitioner has shown by a preponderance of evidence that claims 7, 11, 19, and 21 are *unpatentable*.

B. Related Proceedings

The parties list several cases pending in the Eastern District of Texas that would affect or be affected by the decision in this proceeding, including *Technology Properties Limited, LLC v. Hewlett-Packard Co.*, No. 6:12-cv-208 (E.D. Tex. Mar. 28, 2012), in which the '549 patent is asserted against Petitioner. *See* Pet. 1; Paper 6, 1. On February 11, 2014, after a finding of No Violation of Section 337 in a concurrent proceeding at the International Trade Commission (No. 337-TA-841), a stay of the 6:12-cv-208 case was lifted and it was consolidated with *Technology Properties Limited, LLC v. Cannon, Inc. et al.*, No. 6:12-cv-202 (E.D. Tex. Mar. 28, 2012). A

Markman Hearing is currently scheduled in that case for October 8, 2014. *Technology Properties Limited, LLC v. Cannon, Inc. et al.*, No. 6:12-cv-202 (E.D. Tex. Mar. 14, 2014).

In addition, the '549 patent is the subject of a pending reissue proceeding, US Application 12/351,691. We ordered a stay of that examination pending the termination or completion of this proceeding. Paper 8.

C. The '549 Patent

The '549 patent relates to controllers for flash-memory cards. Ex. 1001, 1:21-22. As described in the "Background of the Invention," at the time of the invention, removable flash-memory cards were commonly used with digital cameras to allow for convenient transfer of images from a camera to a personal computer. *Id.* at 1:26-56. These prior art flash-memory cards were available in several formats, including CompactFlash, SmartMedia, MultiMediaCard (MMC), Secure Digital Card (SD), and Memory Stick card. *Id.* at 2:28-55. Each of the card formats required a different interface adapter to work with a personal computer. *Id.* at 3:9-25.

The Specification describes a need for a flash-memory card reader that accepts flash-memory cards of several different formats using a universal adapter. *Id.* at 3:52-63. In response to this need, the '549 patent describes various improvements to flash-memory card readers, including by determining whether a particular flash-memory card includes a controller and, if not, performing operations to manage error correction for the flash-memory card. *Id.* at 3:24-65.

D. Illustrative Claim

Claim 7, reproduced below, is illustrative of the claimed subject matter:

> 7. A method comprising:
>
> using a controller chip to interface a flash storage system with or without a controller to a computing device, the controller chip comprising a flash adapter, wherein the flash storage system comprises a flash section and at least a medium ID;
>
> determining whether the flash storage system includes a controller for error correction; and
>
> in an event where the flash storage system does not have a controller for error correction, using firmware in the flash adapter to perform operations to manage error correction of the flash section, including bad block mapping of the flash section in the flash storage system that is coupled to the flash adapter section.

II. ANALYSIS

A. Seventh Amendment

As a preliminary matter, MCM argues that *inter partes* review proceedings violate the Seventh Amendment. PO Resp. 2-13. The U.S. Court of Appeals for the Federal Circuit, however, has previously rejected this argument in the context of reexaminations. *Patlex Corp. v. Mossinghoff*, 758 F.2d 594, 603-05 (Fed. Cir. 1985) (holding that even when applied retroactively, the reexamination statute does not violate the jury trial guarantee of the Seventh Amendment); *see also Joy Techs., Inc. v. Manbeck*, 959 F.2d 226, 228-29 (Fed. Cir. 1992) (affirming the holding in *Patlex*), *other grounds superseded by statute*, 35 U.S.C. § 145, *as recognized in In re Teles AG Informationstechnologien*, 747 F.3d 1357 (Fed. Cir. 2014). *Inter partes* review proceedings continue the basic functions of the reexamination proceedings at issue in *Patlex*—authorizing the Office to reexamine the

validity of an issued patent and to cancel any claims the Office concludes should not have been issued. Patent Owner does not identify any constitutionally-significant distinction between reexamination proceedings and *inter partes* review proceedings. Thus, for the reasons articulated in *Patlex*, we conclude that *inter partes* reviews, like reexaminations, comply with the Seventh Amendment.

B. Claim Construction

We construe all terms, whether or not expressly discussed here, using the broadest reasonable construction in light of the '549 patent specification. 37 C.F.R. § 42.100(b). For the purposes of the decision to institute we expressly construed the following terms: (1) "flash adapter" and "flash adapter section" as "a section of the controller chip that enables communication with the flash storage system" and (2) "bad block mapping" as a type of error correction. Decision 5-6. In the post-institution briefs, the parties do not dispute these constructions. *See* Paper 23 ("PO Resp."); Paper 24 ("Reply"). For purposes of this decision, we continue to apply these constructions.

C. Overview of Kobayashi

Kobayashi describes a memory device for a computer with a converter that converts serial commands of the computer to parallel commands that are then used to control a storage medium (which can be a flash-memory card). Ex. 1005, 2:55-64, 3:63-65. This configuration is shown in Figure 1, which is reproduced below.

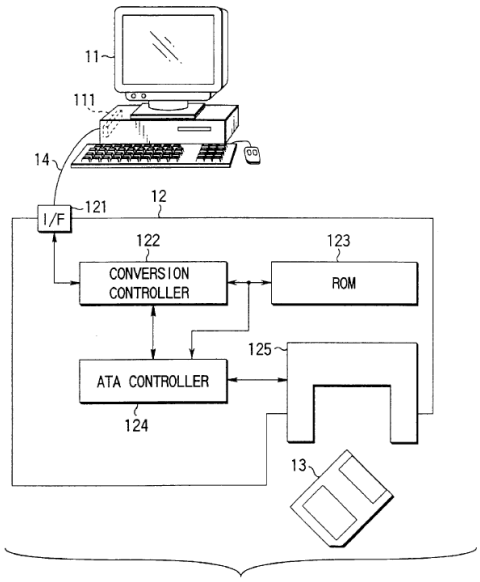


FIG. 1

Figure 1 is a block diagram of computer 11 with reader/writer 12 and flash-memory card 13. *Id.* at 5:54-58. The reader/writer includes conversion controller 122, ATA controller 124, and a connector 125 for reading a flash-memory card 13. *Id.* at 6:5-9.

One of the several embodiments described by Kobayashi is shown in Figure 11, reproduced below.

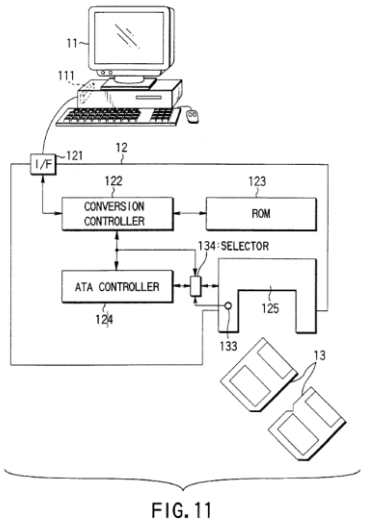


FIG. 11

Figure 11 depicts an embodiment described by Kobayashi. In the embodiment depicted in Figure 11, flash-memory cards 13 both with and without controllers may be used. *Id.* at 12:59-65. Sensor 133 determines the type of flash-memory card 13 mounted on connector 125. *Id.* at 12:59-13: 2. When a flash-memory card with no controller is detected, selector 134 connects ATA controller 124 and connector 125. *Id.* at 13:2-5. When a flash-memory card with a controller is detected, selector 134 connects conversion controller 122 and connector 125.

D. Overview of Kikuchi

Kikuchi describes a flash-memory card and controller 10 having an interface connected to host computer 14. Ex. 1007, Abstract. Figure 1 of Kikuchi is reproduced below.

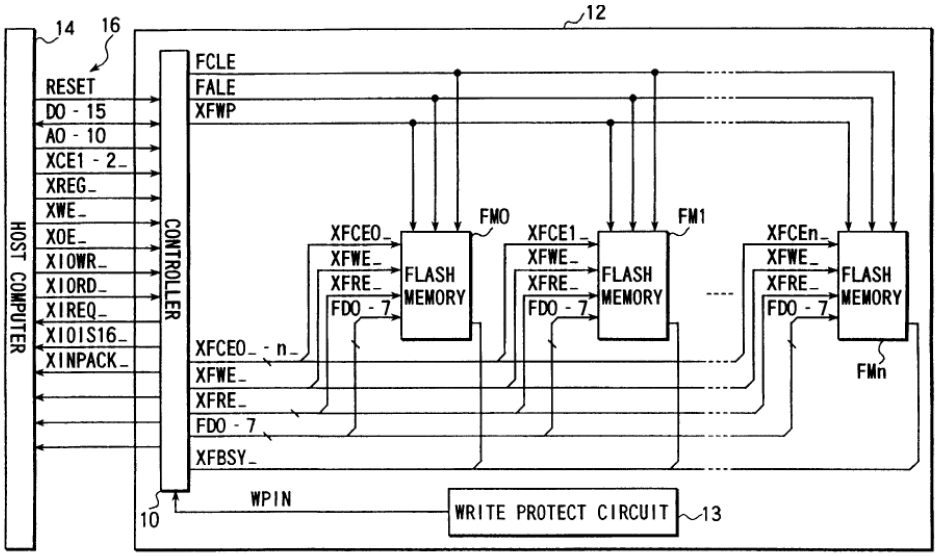
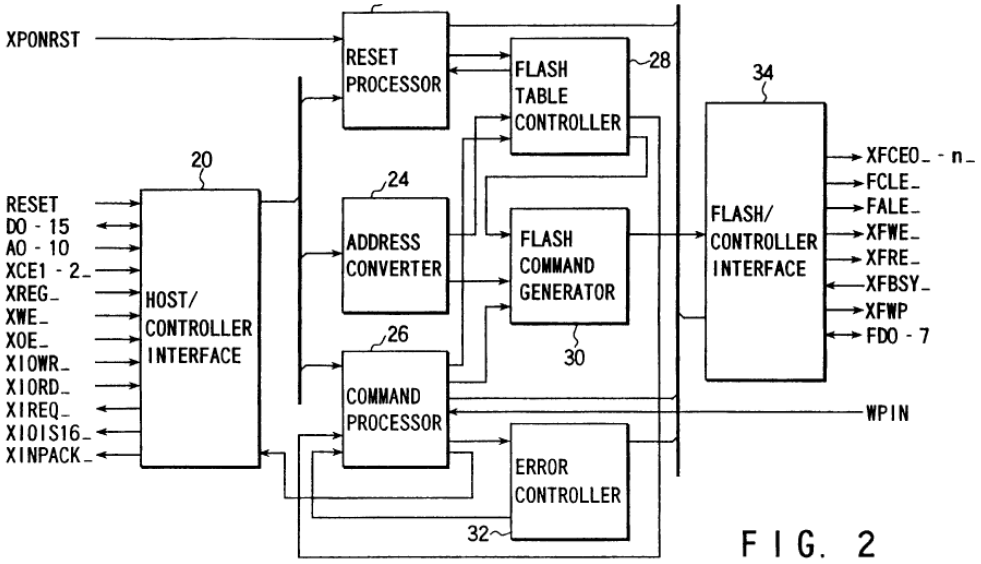


FIG. 1

Figure 1 shows the flash memory card with "one-chip controller" 10 on the flash-memory card. *Id.* at 9:10-15[1]. Figure 2 of Kikuchi is reproduced below.



F I G. 2

Figure 2 is a block diagram showing the functional arrangement of controller 10, including error controller 32, that performs error control for read and write operations. *Id.* at 11:14-20; 13:17-19. Error controller 32 also "performs a block substituting process or the like in the event of a failure or error." *Id.* at 13:17-21. In a separate embodiment, controller 10 "refers to the block quality flag contained in the block status information of the redundant portion of the readout information . . . to check whether the head block BL0 is non-defective or not" and "detects a non-defective block BLj having the highest address rank." *Id.* at 20:20-21:5.

E. Obviousness over Kobayashi and Kikuchi

HP asserts that a person of ordinary skill in the art would have found the challenged claims obvious over the combination of Kobayashi and

[1] In this opinion, page numbers for this exhibit refer to the number at the right hand bottom of the page, not the number in the top middle of the page.

Kikuchi. Pet. 42-57 (citing Ex. 1008 (Declaration of Dr. Sanjay Banerjee) ¶¶ 102-122). In particular, HP asserts that Kobayashi discloses every limitation of the challenged claims except the details of error correction. *Id.* at 47-48. HP relies on Kikuchi as describing the recited error correction. *Id.* at 48-49. In addition, HP asserts that it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of the two references, which both describe ATA controllers that work with flash-memory cards with, or without, on-card controllers, in order to "reliably retain stored data." Pet. 50 (citing Ex. 1008 ¶ 121 (quoting Ex. 1007 (Kikuchi), 4:1-3)).

We are persuaded that a preponderance of the evidence demonstrates that the combination of Kobayashi and Kikuchi discloses each of the limitations of the challenged claims, as presented in HP's Petition. *See* Pet. 42-57; Ex. 1008 ¶¶ 102-122. We are also persuaded that a preponderance of the evidence demonstrates that a person of ordinary skill in the art would have combined the Kobayashi and Kikuchi references. *See* Pet. 50; Ex. 1008 ¶ 121.

MCM explicitly addresses only the requirement of "a controller chip," arguing that Kobayashi does not disclose using a single chip with the claimed functionality, but instead has "multiple chips that perform distinct functions." PO Resp. 14. Specifically, MCM argues that Kobayashi discloses two controllers as separate chips: 122 that exclusively interfaces with cards having controllers, and 124 that exclusively interfaces with cards that do not have controllers. PO Resp. 22. Based on this assertion, MCM argues (1) that the Petition should be dismissed because HP did not point out the single chip requirement explicitly in the Petition (*id.* at 14-21), and

(2) that the combination of Kobayashi and Kikuchi would not yield the claimed invention, which requires a single chip (*id.* at 21-24). We do not find either argument persuasive.

First, we are persuaded that HP sufficiently discussed the single-chip limitation in its Petition. The Petition explicitly points to Kikuchi's disclosure of "controller 10 as a single chip controller." Pet. 49 (citing Ex. 1007, 7:10-22, 9:11-19); *see also* Pet. 48, 53, 55; Ex. 1008 ¶¶ 114-117. Moreover, Petitioner also asserts that "Kobayashi's controller 122 is a 'one-chip microprocessor.'" Pet. 44 (quoting Ex. 1006, 5:66-6:4, 6:12-22); *see also* Pet. 53, 55. These statements, combined with HP's assertion that combining the teachings of the two references is merely "a combination of prior art elements according to known methods to yield predictable results" (Pet. 50-51), were sufficient for us to determine that Petitioner had a reasonable likelihood of showing unpatentability of the challenged claims. Decision 14-16. We are not persuaded otherwise by Patent Owner's post-institution arguments.

Second, this evidence supports a determination that one of ordinary skill in the art would have had both the knowledge and the inclination to place the functionality taught by Kobayashi and Kikuchi on a single chip. *See* Ex. 1007, 7:12-15 ("This flash memory card has a one-chip controller. . . ."); Ex. 1008 ¶¶ 122-23. In fact, MCM conceded at the oral hearing that it was not beyond the skill of one of ordinary skill at the time of the invention to put multiple functions into a single chip and that, in fact, it is common practice to do so.

> JUDGE PERRY: Counsel, are you saying that it is beyond the skill of one of ordinary skill at the time of this invention to put multiple functions integrated into a single chip?

> MR. HELLER: Not at all.
>
> JUDGE PERRY: You are not saying that?
>
> MR. HELLER: Not at all when you have a motivation to do so.
>
> JUDGE PERRY: Isn't it kind of a common practice for those who design integrated circuits to put multiple functions into those circuits?
>
> MR. HELLER: It probably is common practice, but they have to have a motivation to do so.
>
> JUDGE BISK: Is there some reason not to put them on a single chip? It seems like it is just a design choice, whether it is one chip, two chips, 10 chips. Is there a particular reason why the number of chips matters?
>
> MR. HELLER: It is not that. It is, why would you do that? Why would you put all that functionality into a single chip?

Paper 30 ("Tr."), 30:17-31:4.

MCM's assertion—that even if Kikuchi's error correction is incorporated into Kobayashi's ATA controller 124 the result would not yield the claimed invention—misses the point. PO Resp. 20. The relevant inquiry is whether the claimed subject matter would have been obvious to those of ordinary skill in the art in light of the combined teachings of the references. *See In re Keller*, 642 F.2d 413, 425 (CCPA 1981). "Combining the *teachings* of references does not involve an ability to combine their specific structures." *In re Nievelt*, 482 F.2d 965, 968 (CCPA 1973). Patent Owner does not argue that applying the teachings of Kikuchi and Kobayashi so that the claimed functionality is on a single chip would have been "uniquely challenging or difficult for one of ordinary skill in the art" at the time of the invention. *Leapfrog Enters., Inc. v. Fisher-Price, Inc.*, 485 F.3d 1157, 1162 (Fed. Cir. 2007) (citing *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007)).

We conclude that a preponderance of the evidence demonstrates that claims 7, 11, 19, and 21 are unpatentable based on the combination of Kobayashi and Kikuchi.

III. CONCLUSION

Petitioner has shown, by a preponderance of the evidence, that the challenged claims would have been obvious over the combination of Kobayashi and Kikuchi.

Accordingly, it is

ORDERED that claims 7, 11, 19, and 21 of the '549 patent are determined to be *unpatentable*;

FURTHER ORDERED that because this is a final written decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2013-00217
Patent 7,162,549

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Paper 10
Entered: September 10, 2013

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

HEWLETT-PACKARD COMPANY
Petitioner

v.

MCM PORTFOLIO, LLC
Patent Owner

Case IPR2013-00217
Patent 7,162,549

Before SCOTT R. BOALICK, JONI Y. CHANG, and JENNIFER S. BISK, *Administrative Patent Judges.*

BISK, *Administrative Patent Judge*.

DECISION
Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

A. Background

Hewlett-Packard Company ("HP") filed a petition (Paper 2) ("Pet.") to institute an *inter partes* review of claims 7, 11, 19, and 21 of Patent 7,162,549 (the "'549 patent"). 35 U.S.C. § 311. MCM Portfolio, LLC ("MCM") timely filed a Preliminary Response (Paper 9) ("Prelim. Resp."). We conclude that HP has satisfied its burden to show that, under 35 U.S.C. § 314(a), there is a reasonable likelihood that it would prevail with respect to at least one of the challenged claims.

HP contends that the challenged claims are unpatentable under 35 U.S.C. §§102 and/or 103 based on the following specific grounds (Pet. 7):

Reference[s] [1]	**Basis**	**Claims challenged**
AwYong	§ 102	7, 11, 19, and 21
Battaglia	§ 103	7, 11, 19, and 21
Battaglia and the Samaung Datasheet	§ 103	7, 11, 19, and 21
Kobayashi and Kikuchi	§ 103	7, 11, 19, and 21

[1] U.S. Patent 6,987,927 (Ex. 1004) ("Battaglia"); U.S. Patent 6,199,122 (Ex. 1005) ("Kobayashi"); WO 98/03915 (Ex. 1007) ("Kikuchi"); Chee-Kong AwYong, An Integrated Control System Design of Portable Computer Storage Peripherals, Master's Thesis, National Chiao-Tung University, published Dec. 22, 2000 (Ex. 1003) English Translation (Ex. 1002) ("AwYong"); Samsung SmartMedia Card Model No. K9D1208V0M-SSB0 Datasheet (Nov. 20, 2000) (Ex. 1006) ("Samsung Datasheet").

For the reasons described below, we institute an *inter partes* review of claims 7, 11, 19, and 21 based on obviousness over Kobayashi combined with Kikuchi.

We decline to institute *inter partes* review based on the following grounds: (1) anticipation by AwYong; (2) obviousness over Battaglia; and (3) obviousness over Battaglia combined with the Samsung Datasheet.

B. Related Proceedings

The parties list several cases pending in the Eastern District of Texas that would affect or be affected by the decision in this proceeding, including *Technology Properties Limited, LLC v. Hewlett-Packard Co.*, Docket No. 6:12-cv-208 (E.D. Tex. Mar. 28, 2012), in which the '549 patent is asserted against Petitioner. *See* Pet. 1; Paper 6 at 1. That case currently is stayed pending resolution of a related proceeding before the United States International Trade Commission ("ITC") that also involves the '549 patent, ITC Inv. No. 337-TA-841. *Id.* In addition, the '549 patent is the subject of a pending reissue proceeding, U.S. Application No. 12/351,691. The Board ordered a stay of that proceeding pending the termination or completion of this proceeding. Paper 8.

C. The Invention

The '549 patent relates to controllers for flash-memory cards. Ex. 1001, col. 1, ll. 21-22. As described in the "Background of the Invention," at the time of the invention, removable flash-memory cards commonly were used with digital cameras to allow for convenient transfer of images from the camera to a personal computer. *Id.* at col. 1, ll. 26-56. These prior art flash-memory cards were available in several formats, including CompactFlash, SmartMedia, MultiMediaCard (MMC), Secure Digital Card (SD), and Memory Stick card. *Id.* at col. 2, ll. 28-55. Each of the card formats required a different interface adapter

to work with a personal computer. *Id.* at col. 3, ll. 9-25. The Specification describes a need for a flash-memory card reader that accepts flash-memory cards of several different formats using a universal adapter. *Id.* at ll. 52-63. In response to this need, the '549 patent describes various improvements to flash-memory card readers, including by determining whether a particular flash-memory card includes a controller, and if not, performing operations to manage error correction for the flash-memory card. *Id.* at col. 3, l. 53- col. 4, l. 26; col. 28, ll. 42-60.

Claims 7 and 11, reproduced below, are illustrative of the claimed subject matter:

> 7. A method comprising:
>
> using a controller chip to interface a flash storage system with or without a controller to a computing device, the controller chip comprising a flash adapter, wherein the flash storage system comprises a flash section and at least a medium ID;
>
> determining whether the flash storage system includes a controller for error correction; and
>
> in an event where the flash storage system does not have a controller for error correction, using firmware in the flash adapter to perform operations to manage error correction of the flash section, including bad block mapping of the flash section in the flash storage system that is coupled to the flash adapter section.
>
> 11. A system comprising:
>
> a computing device;
>
> a flash storage system comprising a flash section and at least a portion of a medium ID; and
>
> a controller chip coupled between the computing device and the flash storage system to interface the flash storage system to the computing device, the controller chip comprising an interface mechanism capable of receiving flash storage systems with controller and controllerless flash storage systems, a detector to determine whether the flash storage system includes a controller

> for error correction and a flash adapter which comprises firmware to perform, in an event where the flash storage system does not have a controller for error correction, operations to manage error correction of the flash section, including bad block mapping of the flash section in the flash storage system that is coupled to the flash adapter section.

D. Claim Construction

As a step in our analysis for determining whether to institute a trial, we determine the meaning of the claims. Consistent with the statute and the legislative history of the AIA, the Board will interpret claims using the broadest reasonable construction. *See* 37 C.F.R. § 42.100(b); *Office Patent Trial Practice Guide*, 77 Fed. Reg. 48756, 48766 (Aug. 14, 2012).

1. "Flash Adapter" and "Flash Adapter Section"

HP proposes that the broadest reasonable construction of "flash adapter" and "flash adapter section" is that adopted in the related ITC Investigation—"a section of the controller chip that enables communication with the flash storage system." Pet. 8 (citing Ex. 1030, pp. 73-77). MCM agrees with that construction. Prelim. Resp. 11. We find that this definition is reasonable and supported by the claim language, and thus adopt this definition for purposes of this decision.

2. "Error Correction" and "Bad Block Mapping"

HP does not set forth an explicit construction for the terms "error correction" or "bad block mapping." MCM, however, argues that HP incorrectly construes the term "bad block mapping" as distinct from "error correction." Prelim. Resp. 11. (citing Ex. 1008 ("Banjeree Decl.") ¶ 28). MCM instead proposes a construction of the term used by the examiner during original prosecution—"bad block mapping is a form of error correction." Prelim. Resp. 11-12 (citing Ex. 1015 at 415).

"Bad block mapping" is not defined explicitly in the written description of

the '549 patent. The plain and ordinary meaning of "bad block" is "a faulty memory location." MICROSOFT COMPUTER DICTIONARY 41 (4th ed. 1999). The plain and ordinary meaning of "a memory map" is "a description of the layout of objects in an area of memory." *Id.* at 281. Thus, the plain and ordinary meaning of "bad block mapping" is a description of the layout of those faulty memory locations, kept so that they are not accessed. Under a broadest reasonable construction, bad block mapping is thus a type of error correction.

This construction also is consistent with the Specification, which states that "the primary reason for including a controller section in a flash medium is for error correction. This task is now shifted either to firmware 4012*b* of the host computer, which now on top of its normal access section software, also manages error correction and bad block mapping of chip(s) 4022 and stores those parameters in flash medium 4020*b* itself." Ex. 1001, col. 28, ll. 53-58. This is the only place, outside the claims, that the term "bad block mapping" is used in the '549 patent. However, the claim language also supports this construction. Claim 7 recites "using firmware in the flash adapter to perform operations to manage error correction of the flash section, including bad block mapping of the flash section," and claim 11 recites "operations to manage error correction of the flash section, including bad block mapping of the flash section."

For these reasons, for purposes of this decision, we construe the term "bad block mapping" to be a type of "error correction."

II. ANALYSIS

A. 35 U.S.C. § 315(b)

MCM argues that institution of an *inter partes* review is barred under 35 U.S.C. § 315(b).[2] Section 315(b) states as follows:

> An inter partes review may not be instituted if the petition requesting the proceeding is filed more than 1 year after the date on which the petitioner, real party in interest, or privy of the petitioner is served with a complaint alleging infringement of the patent.

MCM asserts that Pandigital, Inc. is a privy of HP and, therefore, a complaint served on Pandigital by MCM in 2011, more than one year prior to the filing of the Petition in this case, filed by HP on March 27, 2012, should trigger § 315(b). Prelim. Resp. 5 (citing Ex. 2001 (*Technology Properties Limited LLC v. Pandigital, Inc.*, No. 2:11-cv-00372-TJW (E.D. Tex. 2011) (the "Texas Action"))). MCM bases this allegation on the fact that HP resells Pandigital products accused of infringing the '549 patent in the Texas Action. *Id.* at 5-6 (citing Ex. 2003 at 20 (HP User Guide)). According to MCM, the Petition in this case is filed more than one year after service of the complaint on Pandigital, a privy of HP. Prelim. Resp. 5-9.

MCM does not provide persuasive evidence that HP and Pandigital are privies for purposes of § 315(b). "Whether a party who is not a named participant in a given proceeding nonetheless constitutes a 'real party-in-interest' or 'privy' to that proceeding is a highly fact-dependent question." *Office Patent Trial Practice Guide*, 77 Fed. Reg. 48759 (citing *Taylor*, 553 U.S. 880). "The Office intends to

[2] MCM asserts that HP "lacks standing" to bring this IPR. Standing technically is not a requirement in an IPR. *See, e.g., Office Patent Trial Practice Guide*, Fed. Reg. at 48759 ("[The notion of 'real party-in-interest'] reflects standing concepts, but no such requirement exists in the IPR or PGR context.").

evaluate what parties constitute 'privies' in a manner consistent with the flexible and equitable considerations established under federal caselaw." *Id.* Petitioner provides no persuasive evidence that HP could have exercised control over Pandigital's participation in the Texas Action. Thus, § 315(b) does not bar institution of *inter partes* review based on HP's Petition.

MCM bases its privity argument solely on its assertion that HP and Pandigital are successive owners of the same allegedly infringing property. Prelim. Resp. 7 (citing *Taylor v. Sturgell*, 553 U.S. 880, 894 (2008)). We are not persuaded that this allegation alone is enough to confer privity for purposes of § 315(b). *See Synopsys v. Mentor Graphics Corp.*, IPR2012-00042, Decision to Institute, Paper 16 (Feb. 22, 2013) ("*Synopsis*"). Under *Synopsis* "any potentially infringing products are irrelevant to the issues raised in the Petition, all of which involve patentability." *Synopsis* at 17.

B. Priority Date for the '549 Patent Claims

The '549 patent claims the benefit of one provisional application and is a continuation-in-part of four non-provisional applications. Ex. 1001, col. 1, ll. 6-17; Certificate of Correction (Jan. 9, 2007). MCM asserts that the effective filing date of the challenged claims is the earliest filing date of these applications—application No. 09/610,904, filed July 6, 2000 (now U.S. Patent 6,438,638) (the "'904 application"). Prelim. Resp. 17-18. HP, on the other hand, asserts that the challenged claims are entitled to an effective filing date no earlier than June 4, 2002. Pet. 3.

In this case, the effective filing date of the '549 patent (i.e., whether it is entitled to the benefit of the '904 application's filing date) is relevant because several of the asserted references post-date the filing date of the '904 application. In particular, although AwYong is stamped with a date of June 2000, HP states that

it was "published and publicly available as of December 22, 2000," several months after the filing of the '904 application. In addition, Battaglia has a filing date of July 13, 2000, and HP states that the Samsung Datasheet was available by November 20, 2000—both of which are after the '904 application's filing date.

HP provides little explanation regarding its proposed effective date, basing its entire argument on the statement that "[i]n the related ITC Investigation, the Patent Owner's exclusive licensee – Technology Properties Limited, LLC ('TPL') – agreed that June 4, 2002 is the effective filing date of the '549 Patent." Pet. 3 (citing Ex. 1008 ("Banerjee Decl.") ¶ 33). HP does not explain why the actions of MCM's licensee in another proceeding would be applicable here; nor does HP provide any evidence, aside from one conclusory statement by an expert, Dr. Banerjee, to support this assertion. *Id.*

Other than the conclusory statement regarding the related ITC Investigation, we find no other evidence in the record[3] to support the proposed 2002 effective date except the testimony of Dr. Banerjee, who states that "Claims 7, 11, 19, and 21 of the '549 Patent are entitled to a priority date of no earlier than June 4, 2002" because the concepts of interfacing with "intelligent" and "dumb" flash cards do not appear until a provisional application on June 4, 2002. Ex. 1008 ¶¶ 33-34. HP, however, does not provide any of the underlying evidence upon which these conclusions are based. We, therefore, give them minimal weight. 37 C.F.R. § 42.65. None of the applications to which the '549 patent claims benefit have been entered into the record in this case. Moreover, Dr. Banerjee's statement does not refer to all those applications. Specifically, Dr. Banerjee does not mention the

[3] HP did not cite to any other testimony in its Petition, but MCM does refer to other testimony by disputing that testimony in its response. Prelim. Resp. 17-18.

'904 application, included in the certificate of correction, which has the earliest filing date—July 6, 2000; instead, he specifically discusses only the applications listed in the first column of the '549 patent. *Id.* at ¶ 34. Thus, it is unclear from the testimony whether Dr. Banerjee studied or was aware of the earliest claimed application.

Because we are not persuaded by HP's contention that the challenged claims are not entitled under 35 U.S.C. § 120 to the benefit of the filing date of the '904 application, HP has not shown sufficiently that AwYong, Battaglia, or the Samsung Datasheet are eligible as prior art for purposes of this decision. Thus, we decline to institute *inter partes* review based on any of those references.

C. Obviousness over Kobayashi and Kikuchi

HP argues that claims 7, 11, 19, and 21 of the '549 patent are obvious over Kobayashi combined with Kikuchi. Both Kobayashi and Kikuchi pre-date the filing date of the '904 application. Kobayashi is a U.S. patent that was filed July 22, 1998 and Kikuchi is a PCT application published January 29, 1998.

1. Kobayashi

Kobayashi describes a memory device for a computer with a converter that converts serial commands of the computer to parallel commands that then are used to control a storage medium (which can be a flash-memory card). Ex. 1005, col. 2, ll. 55-64; col. 3, ll. 63-65. This configuration is shown in Figure 1.

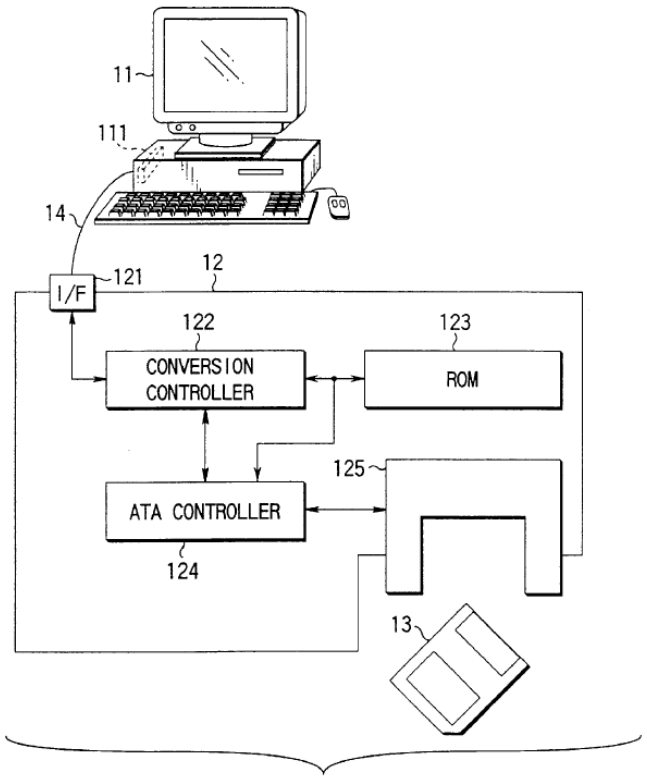


FIG. 1

Figure 1 of Kobayashi, reproduced above, is a block diagram of a computer 11 with a reader/writer 12 and flash-memory card 13. Ex. 1005, col. 5, ll. 54-58. The reader/writer includes a conversion controller 122, an ATA (AT Attachment) controller 124, and a connector 125 for reading a flash-memory card 13. *Id.* at col. 6, ll. 5-9. In the first of several embodiments described by Kobayashi, the flash-memory card 13 does not have a controller on the card. *Id.* at col. 6, ll. 1-4 ("The memory card 13 functions as what is called a silicon disk or a PC card according to the ATA standard, and stores data and reads, outputs and erases the stored data under an *external control*.") (emphasis added). A second embodiment described by Kobayashi includes a flash-memory card 13 with a controller arranged in the memory card. *Id.* at col. 12, ll. 44-46, 59-63. A third embodiment is shown in Figure 11.

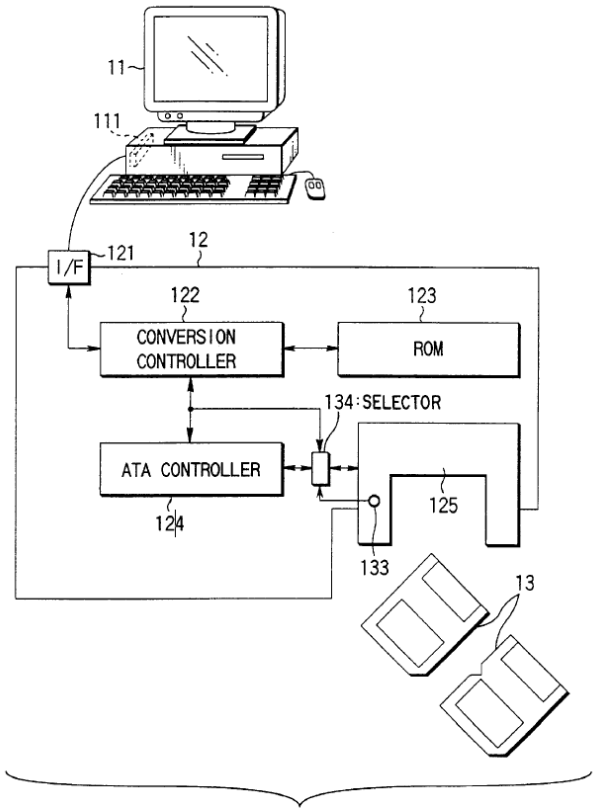


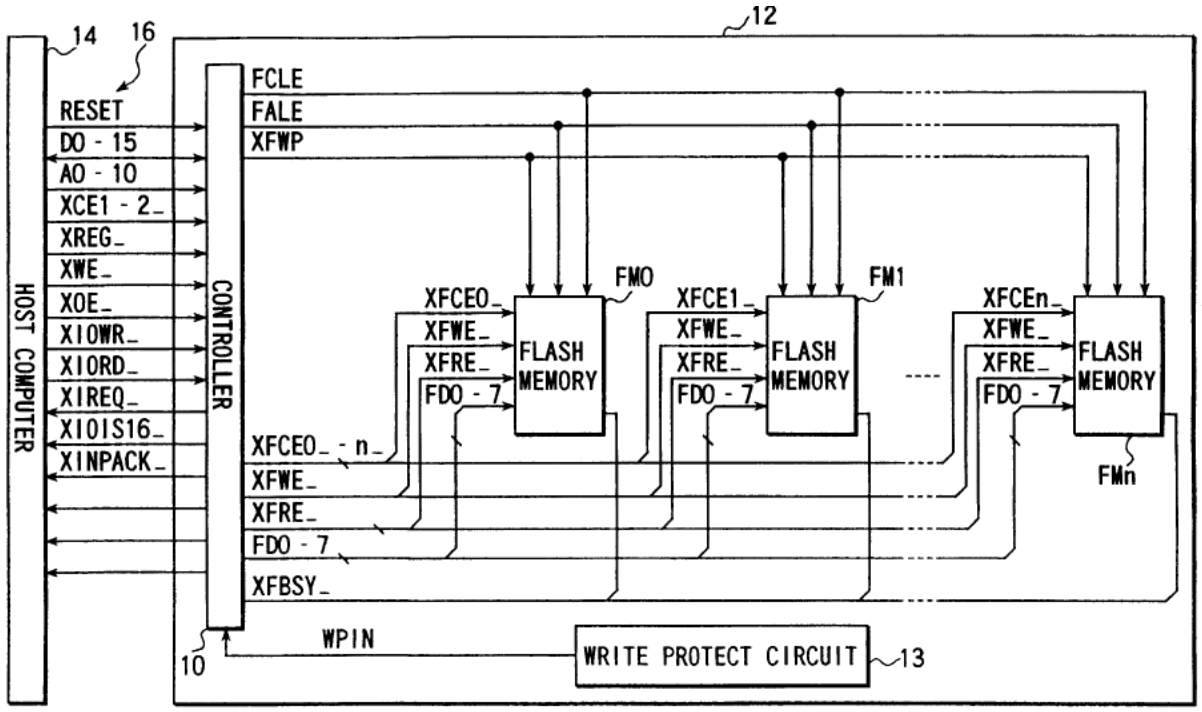
FIG. 11

In this third embodiment, flash-memory cards 13 both with and without controllers may be used. *Id.* at col. 12, ll. 59-65. A sensor 133 determines the type of flash-memory card 13 mounted on the connector 125. *Id.* at col. 12, l. 59 – col. 13, l. 2. When a flash-memory card with no controller is detected, a selector 134 connects the ATA controller 124 and the connector 125. *Id.* at col. 13, ll. 2-5. When a flash-memory card with a controller is detected, a selector 134 connects the conversion controller 122 and the connector 125.

2. Kikuchi

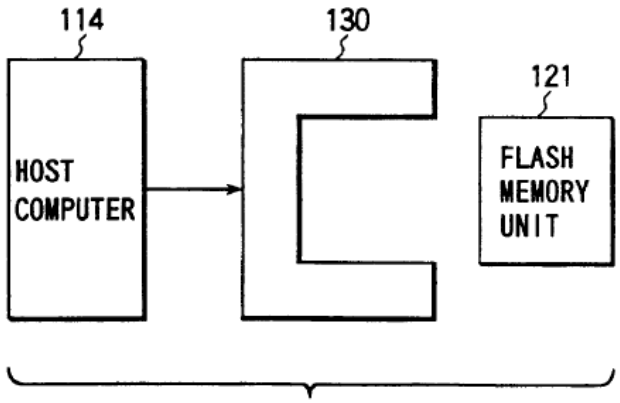
Kikuchi describes a flash-memory card and a controller 10 having an interface connected to a host computer 14. Ex. 1007, Abstract. Figure 1 of Kikuchi, reproduced below, shows the flash memory card with a controller on the

flash-memory card. *Id.* at p. 9, ll. 10-15.



F I G. 1

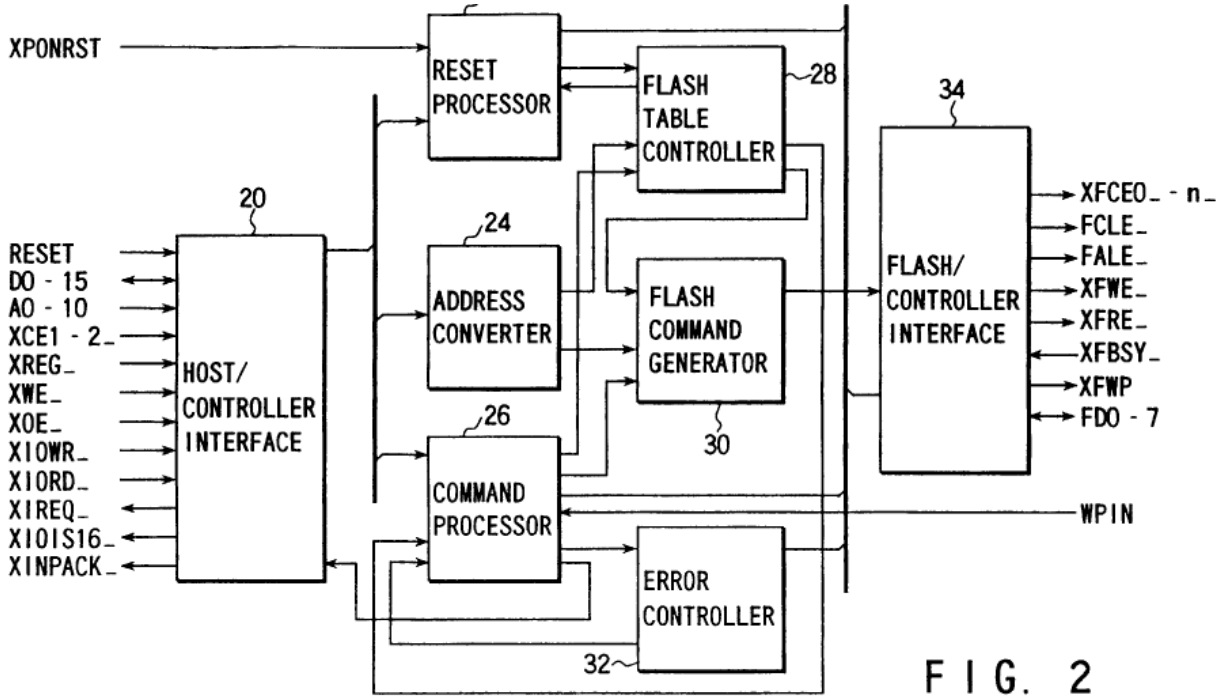
Figure 15A of Kikuchi, reproduced below, shows a flash-memory card with no controller. Ex. 1007, p. 33, ll. 22-25.



F I G. 15B

Figure 2, reproduced below, is a block diagram showing the functional

arrangement of the controller 10.



F I G. 2

In Figure 2, above, the error controller 32 performs error control in read and write operations and performs bad block mapping, for example, "a block substitute process or the like in the event of a failure or error." Ex. 1007, p. 13, ll. 17-21. Further, in another embodiment, controller 10 "refers to the block quality flag contained in the block status information of the redundant portion of the readout information . . . to check whether the head block BL0 is non-defective or not" and "detects a non-defective block BLj having the highest address rank." *Id.* at p. 22, l. 20 – p. 23, l. 5.

3. The Combination of Kobayashi and Kikuchi

HP asserts that Kobayashi discloses every limitation recited by all the challenged claims, except that HP concedes that Kobayashi is silent on the details of how error correction is performed and, in particular, does not mention bad block mapping. Pet. 47-48. HP relies on Kikuchi for teaching the details of error

correction, including bad block mapping, done in firmware. Pet. 48-50. HP contends that it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of the two references, which both describe ATA controllers that work with flash-memory cards with or without on-card controllers, in order to "reliably retain stored data." Pet. 50 (citing Banerjee Decl. ¶ 121 (quoting Ex. 1007 (Kikuchi), p. 6, ll. 1-3)). We have reviewed HP's evidence in relation to each of the challenged claims and find that the evidence supports HP's contentions.

MCM argues that Kobayashi does not disclose using firmware to perform the error correction in the event that the flash-memory card is without a controller, as required by all the challenged claims. Prelim. Resp. 29. This argument is not persuasive because MCM concedes that Kikuchi discloses a controller using firmware to perform error correction. *Id.* at 29-31 (stating that Kikuchi discloses "a controller in a card reader that has a microprocessor that conducts bad block mapping in firmware").

MCM argues that Kikuchi's controller chip could not be incorporated into Kobayashi's controller. Prelim. Resp. 31-32. Moreover, MCM adds that even if Kikuchi's controller chip could be incorporated into Kobayashi's controller, it would not yield the claimed invention because Kobayashi discloses two controllers—a conversion controller 122 and an ATA controller 124—not one controller chip with all the required functionality. Prelim. Resp. 33-34.

Neither argument is persuasive. "It is well-established that a determination of obviousness based on teachings from multiple references does not require an actual, physical substitution of elements." *In re Mouttet*, 686 F.3d 1322, 1332 (Fed. Cir. 2012) (citing *In re Etter*, 756 F.2d 852, 859 (Fed. Cir. 1985) (en banc) (noting that the criterion for obviousness is not whether the references can be

combined physically, but whether the claimed invention is rendered obvious by the teachings of the prior art as a whole)). On this record, we determine that the petition and supporting evidence demonstrate sufficiently that combining the teachings of Kobayashi and Kikuchi merely is a predictable use of prior art elements according to their established functions—an obvious improvement. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007).

Finally, MCM argues that Kobayashi was considered by the Examiner during prosecution (Prelim. Resp. 25) and Kikuchi is cumulative of art that was before the Examiner during prosecution (Prelim. Resp. 29-30). While we are mindful of the burden on MCM and the Office in analyzing previously considered prior art, substantially the same prior art and arguments were not before the Office previously. *See* 35 U.S.C. § 325(d). Moreover, for the reasons explained above, we conclude that HP's arguments based on the combination of Kobayashi and Kikuchi have merit.

III. CONCLUSION

We institute an *inter partes* review of claims 7, 11, 19, and 21 based on obviousness over Kobayashi combined with Kikuchi.

IV. ORDER

For the reasons given, it is

ORDERED that the Petition is granted as to claims 7, 11, 19, and 21 of the '549 patent on the alleged ground of obviousness over Kobayashi combined with Kikuchi under 35 U.S.C. § 103.

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(a), *inter partes* review of the '549 patent hereby is instituted commencing on the entry date of this Order, and pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice

hereby is given of the institution of a trial.

FURTHER ORDERED that an initial conference call with the Board is scheduled for **2 PM Eastern Time** on **October 9, 2013**. The parties are directed to the *Office Trial Practice Guide*, 77 Fed. Reg. at 48765-66 for guidance in preparing for the initial conference call, and should come prepared to discuss any proposed changes to the Scheduling Order entered herewith and any motions the parties anticipate filing during the trial.

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Paper 19
Entered: October 10, 2013

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

HEWLETT-PACKARD COMPANY
Petitioner

v.

TECHNOLOGY PROPERTIES LIMITED LLC,
and MCM PORTFOLIO LLC
Exclusive Licensee and Patent Owner

Case IPR2013-00217
Patent 7,162,549

Before JONI Y. CHANG, GLENN J. PERRY, and JENNIFER S. BISK, *Administrative Patent Judges.*

BISK, *Administrative Patent Judge*.

DECISION
Request for Rehearing
37 C.F.R. § 42.71(d)

SUMMARY

Patent Owner, MCM Portfolio LLC ("MCM"), requests rehearing of the Board's decision (Paper 10) ("Decision"), entered September 10, 2013, instituting *inter partes* review of claims 7, 11, 19, and 21 of U.S. Patent 7,162,549 (Ex. 1001). Paper 13 ("Rehearing Req."). For the reasons that follow, MCM's request for rehearing is *denied.*

DISCUSSION

The applicable standard for granting a request for rehearing is abuse of discretion. The requirements are set forth in 37 C.F.R. § 42.71(d), which provides in relevant part:

> A party dissatisfied with a decision may file a request for rehearing, without prior authorization from the Board. The burden of showing a decision should be modified lies with the party challenging the decision. The request must specifically identify all matters the party believes the Board misapprehended or overlooked, and the place where each matter was previously addressed in a motion, an opposition, or a reply.

MCM argues that a Federal Circuit decision issued subsequent to the filing of the Preliminary Response (Paper 9, filed June 28, 2013) requires the Board to reconsider its decision that 35 U.S.C. § 315(b) does not bar institution of *inter partes* review based on HP's Petition. Rehearing Req. 3. Specifically, the Board determined that MCM's assertion that HP and Pandigital are successive owners of the same allegedly infringing property was not enough to support the existence of privity between HP and Pandigital for purposes of § 315(b). Decision 7-8.

In its Request for Rehearing, MCM argues that the Federal Circuit's August 29, 2013, decision in *Aevoe Corporation v. AE Tech Company, LLC,* mandates that *inter partes* review not be instituted. Rehearing Req. 3-4 (citing *Aevoe Corp. v. AE Tech Co.*, 2013 WL 4563014 (Fed. Cir. 2013)). In particular,

MCM suggests that *Aevoe* requires the Board to consider, on the issue of privity, MCM's notice to HP that HP's sales of products manufactured by Pandigital were infringing MCM's patent and the subsequent notice to HP of the Texas Action against Pandigital involving those products. Rehearing Req. 3-4.

We do not agree that *Aevoe* requires a reconsideration of our decision regarding lack of privity. *Aevoe* involves an order that enjoined AE Tech and its agents from the "making, manufacturing, importing, offering for sale, selling, and/or otherwise using" a particular patent. *Aevoe*, 2013 WL 4563014 at *3. Thus, the privity relationship at issue in that case was one related to the infringing products and the reach of the governing injunction. *Id.* at *8 ("[B]y virtue of their distribution agreement, the S&F Defendants were 'privies' of AE Tech, did not act independently of AE Tech, and were, thus, subject to the original injunction. *See Golden State Bottling Co.* 414 U.S. at 179, 94 S. Ct. 414 (stating that a purchaser acquiring property with knowledge that the wrong enjoined remained unremedied is considered in privity for purposes of Rule 65(d)).").

As we have explained, privity is a contextual concept. *Synopsys v. Mentor Graphics Corp.*, IPR2012-00042, Decision to Institute, Paper 16 at 17 (Feb. 22, 2013). The facts and circumstances present in *Aevoe* are not present here. The allegedly infringing products referred to by MCM are not at issue in this proceeding. Thus, we are not persuaded that *Aevoe* requires that we reconsider our decision that MCM has failed to show that HP and Pandigital are privies for purposes of this proceeding.

MCM makes several other arguments relating to the issue of privity and the § 315(b) bar, but does not identify any arguments or evidence that it asserts the

Board misapprehended or overlooked.[1] *See* Rehearing Req. 9-15; 37 C.F.R. § 42.71(d). A request for rehearing is not an opportunity to express disagreement with a decision.

MCM's request for rehearing is *denied.*

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[1] We agree with MCM that there is a typographical error on page 8 of the Decision. The sentence "*Petitioner* provides no persuasive evidence that HP could have exercised control over Pandigital's participation in the Texas Action" should read "*Patent Owner* provides no persuasive evidence that HP could have exercised control over Pandigital's participation in the Texas Action." Decision 8 (emphases added). However, this does not change the outcome of either the Decision or this decision on request for rehearing. An errata correcting the typographical error will be issued simultaneously with this decision.

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Paper 20
Entered: October 20, 2013

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

HEWLETT-PACKARD COMPANY
Petitioner

v.

TECHNOLOGY PROPERTIES LIMITED LLC,
and MCM PORTFOLIO LLC
Exclusive Licensee and Patent Owner

Case IPR2013-00217
Patent 7,162,549

ERRATA

There is a typographical error on page 8 of the Decision issued on September 10, 2013 as Paper 10. The sentence "*Petitioner* provides no persuasive evidence that HP could have exercised control over Pandigital's participation in the Texas Action" should read "*Patent Owner* provides no persuasive evidence that HP could have exercised control over Pandigital's participation in the Texas Action."

/Amy Kattula/
Paralegal Specialist

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US007162549B2

(12) **United States Patent**
Mambakkam et al.

(10) **Patent No.: US 7,162,549 B2**
(45) **Date of Patent: Jan. 9, 2007**

(54) **MULTIMODE CONTROLLER FOR INTELLIGENT AND "DUMB" FLASH CARDS**

(75) Inventors: **Sreenath Mambakkam**, San Jose, CA (US); **Larry Lawson Jones**, Palo Alto, CA (US); **Arockiyaswamy Venkidu**, Menlo Park, CA (US); **Nicholas Antonopoulos**, San Jose, CA (US)

(73) Assignee: **Onspec Electronics, Inc.**, Cupertino, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/264,466**

(22) Filed: **Oct. 4, 2002**

(65) **Prior Publication Data**

US 2003/0093606 A1 May 15, 2003

Related U.S. Application Data

(63) Continuation-in-part of application No. 10/063,021, filed on Mar. 12, 2002, and a continuation-in-part of application No. 10/002,567, filed on Nov. 1, 2001, now abandoned, and a continuation-in-part of application No. 10/039,685, filed on Oct. 29, 2001, now Pat. No. 6,832,281.

(60) Provisional application No. 60/386,396, filed on Jun. 4, 2002.

(51) **Int. Cl.**

G06F 3/00	(2006.01)
G06F 13/00	(2006.01)
G06F 11/00	(2006.01)
G11C 29/00	(2006.01)

(52) **U.S. Cl.** **710/16**; 710/8; 710/17; 710/19; 710/74; 714/1; 714/42; 714/773

(58) **Field of Classification Search** 710/63, 710/62, 65, 72–74, 8, 12; 714/1, 42, 773
See application file for complete search history.

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Primary Examiner—Kim Huynh
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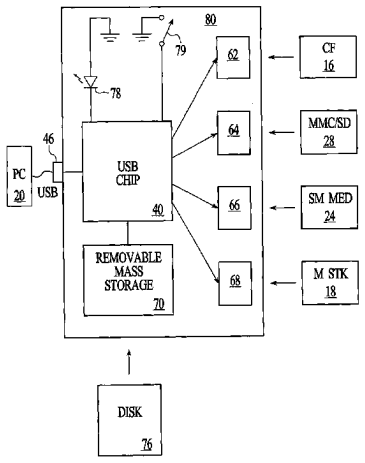
(74) *Attorney, Agent, or Firm*—Greenberg Traurig, LLP; John P. Ward

(57) **ABSTRACT**

A controller chip for coupling a computer system with a flash storage system is disclosed. The controller chip comprises an interface mechanism for determining whether the Flash storage system includes a controller and an adapter for providing the appropriate interface to the computer system to allow the computer system to communicate with the Flash storage system. In a preferred embodiment, the flash storage system comprising at least a portion of a medium ID section; and a flash section, wherein the medium ID section contains specifications of the medium ID. Through the use of this system a plurality of different adapters and a flash storage system can be managed while utilizing the same hardware components.

22 Claims, 35 Drawing Sheets



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6,330,688	B1 *	12/2001	Brown	714/7
6,353,870	B1	3/2002	Mills et al.	
6,405,323	B1	6/2002	Lin et al.	
6,408,352	B1	6/2002	Hosaka et al.	
6,438,638	B1 *	8/2002	Jones et al.	710/301
2001/0014934	A1	8/2001	Toba	
2002/0111771	A1 *	8/2002	Huang et al.	702/186
2002/0185533	A1 *	12/2002	Shieh et al.	235/441
2003/0038177	A1 *	2/2003	Morrow	235/441
2003/0041203	A1 *	2/2003	Jones et al.	710/301
2003/0041284	A1 *	2/2003	Mambakkam et al.	714/15
2003/0046469	A1	3/2003	Liu et al.	
2003/0084220	A1	5/2003	Jones et al.	
2003/0084221	A1 *	5/2003	Jones et al.	710/302
2003/0093606	A1 *	5/2003	Mambakkam et al.	710/305
2004/0027879	A1 *	2/2004	Chang	365/200

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WO	WO 00/23936	*	4/2000

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* cited by examiner

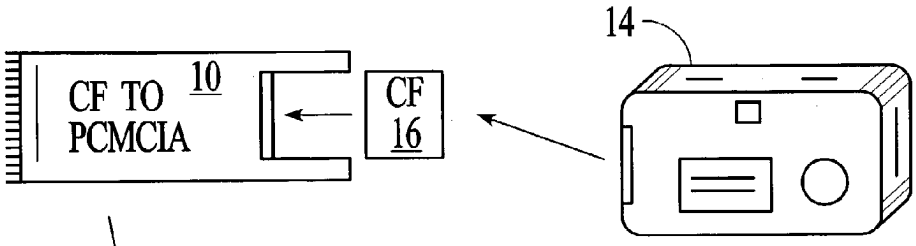


FIG. 1A (PRIOR ART)

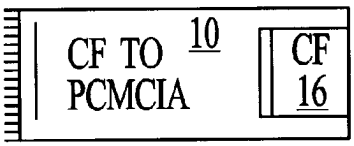


FIG. 1B (PRIOR ART)

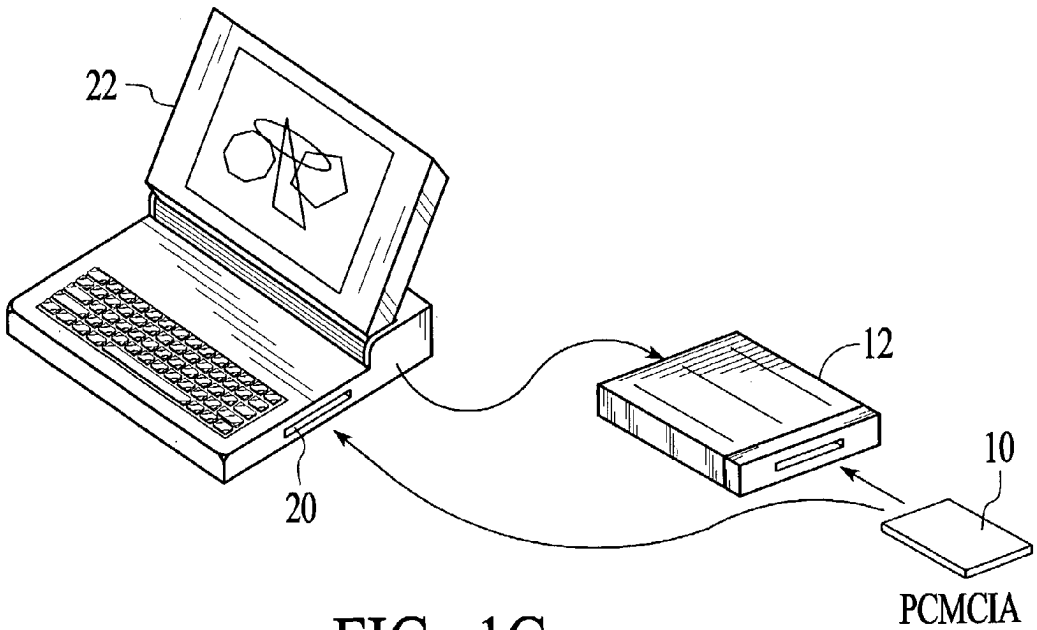


FIG. 1C (PRIOR ART)

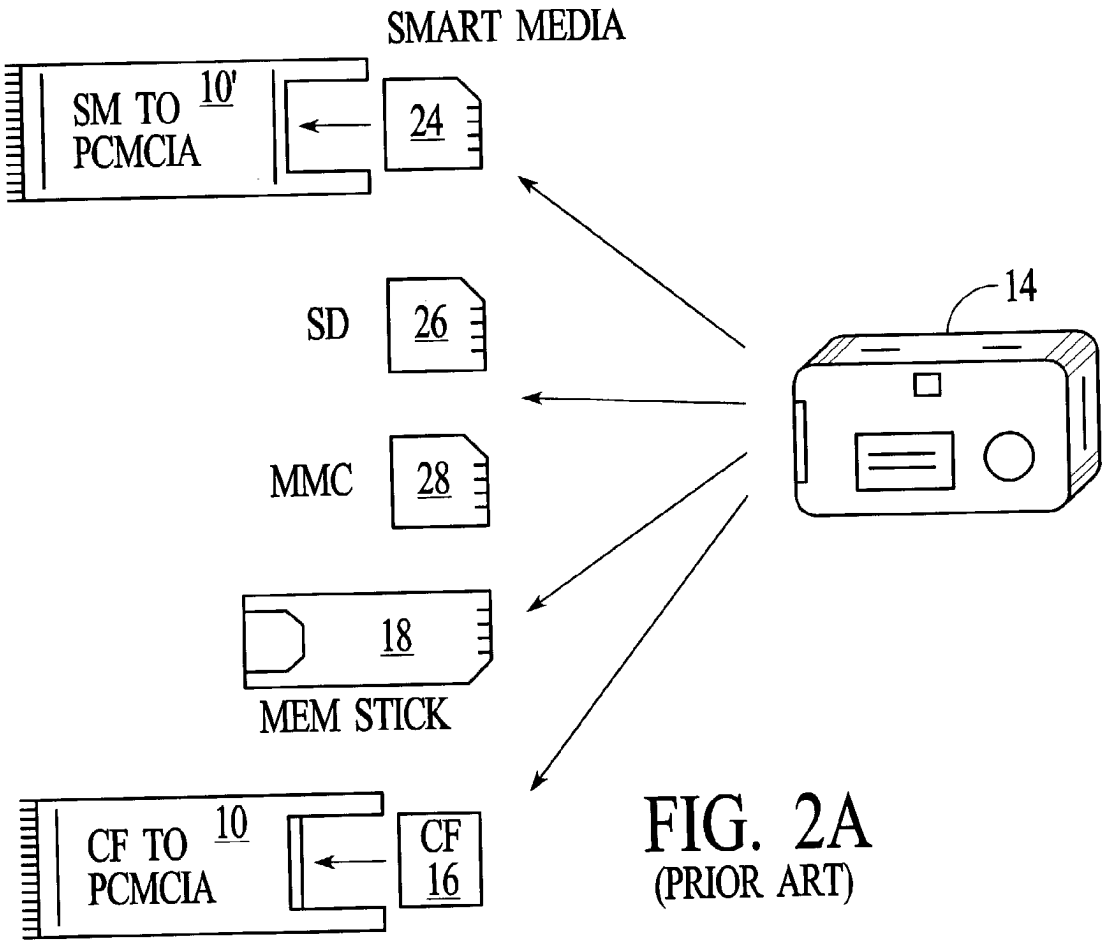


FIG. 2A
(PRIOR ART)

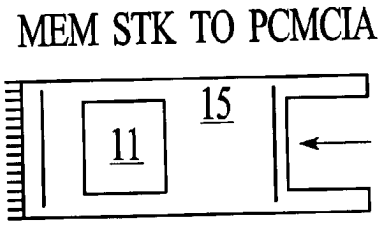
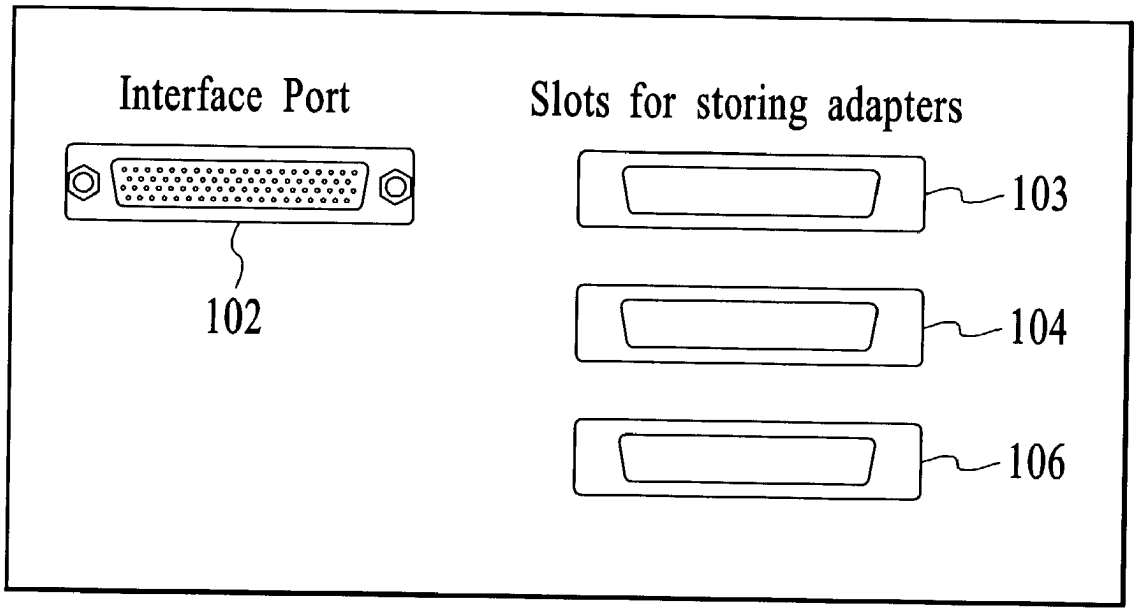


FIG. 2B



100

FIG. 2C

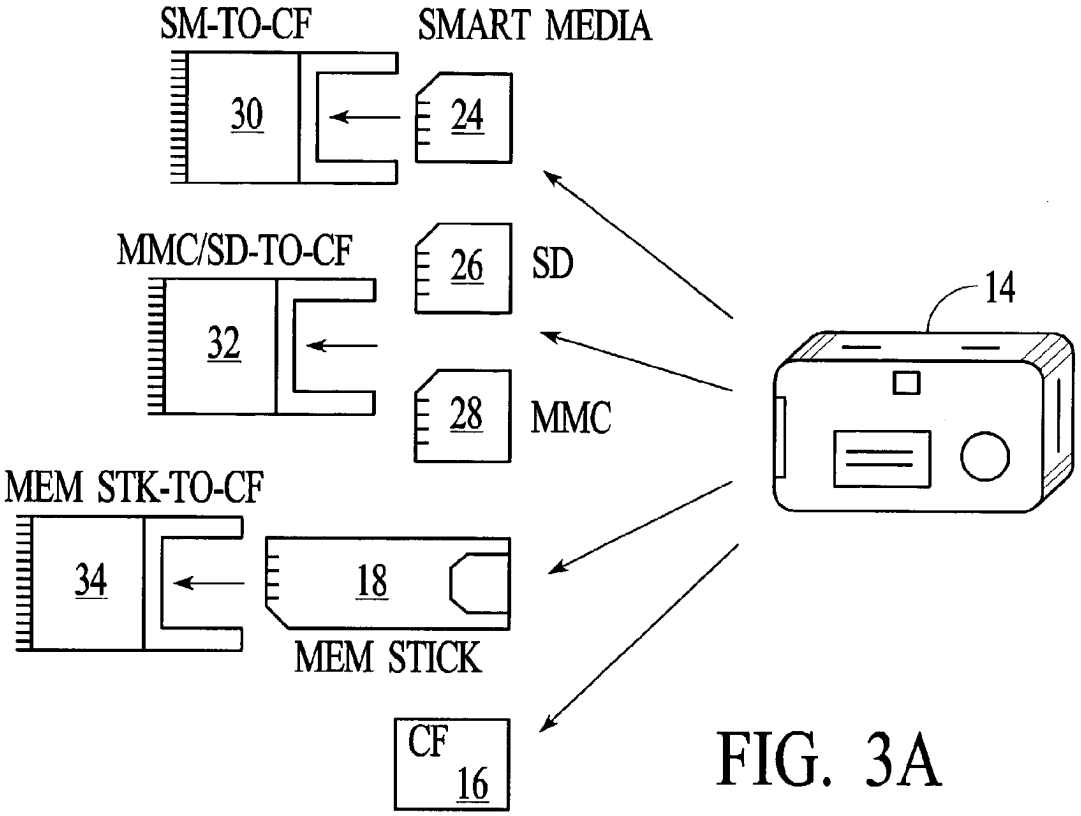

SM-TO-CF
SMART MEDIA
30
24
MMC/SD-TO-CF
26
SD
32
28
MMC
14
MEM STK-TO-CF
34
18
MEM STICK
CF
16

FIG. 3A

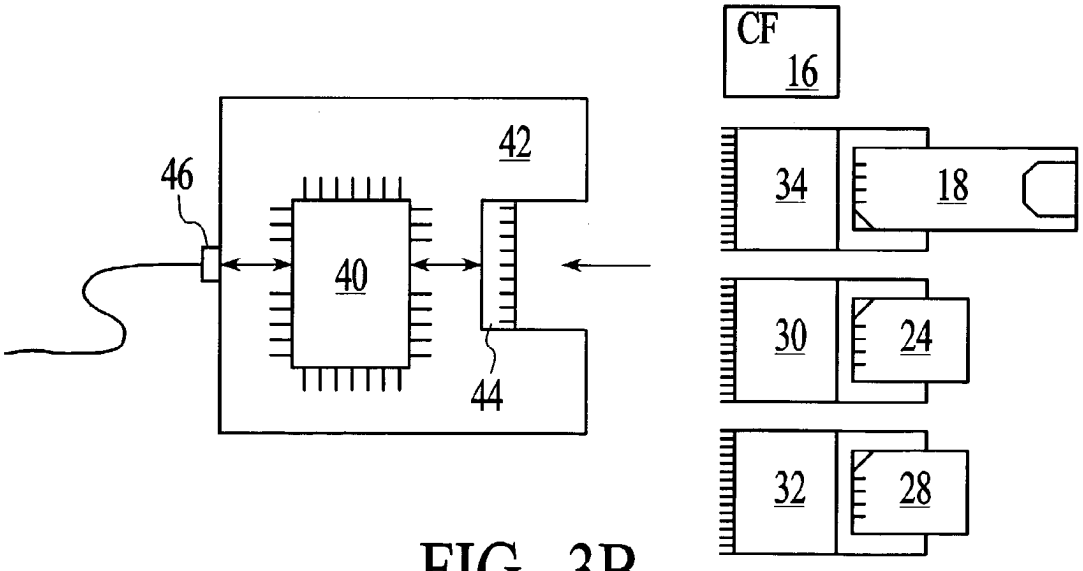

CF
16
42
46
40
44
34
18
30
24
32
28

FIG. 3B

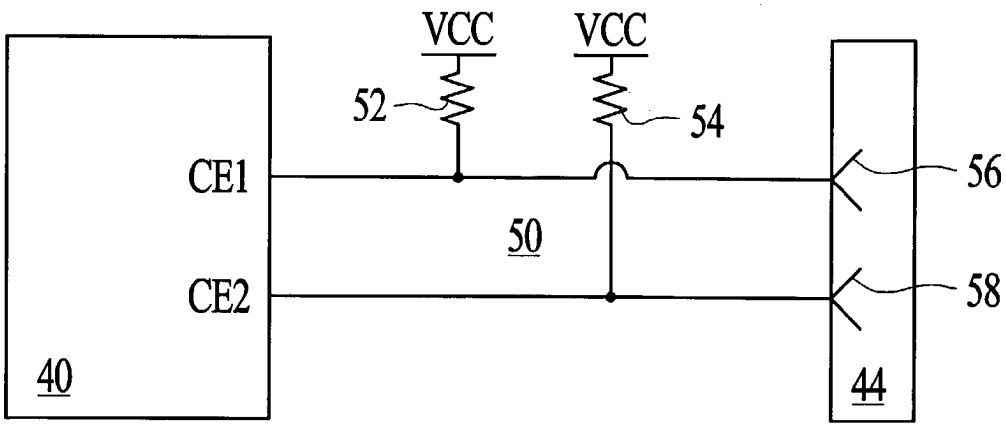

VCC
VCC
52
54
CE1
50
CE2
56
58
40
44

FIG. 4A

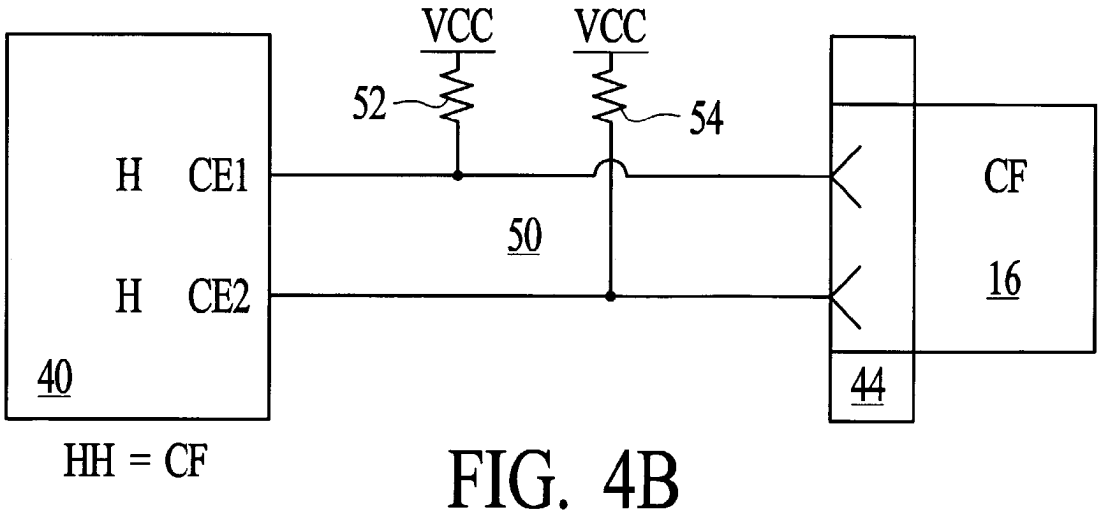
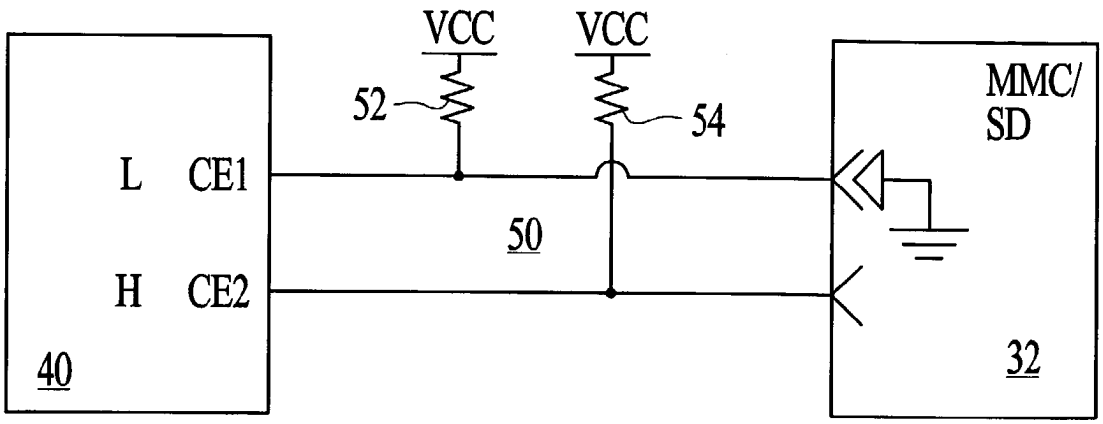
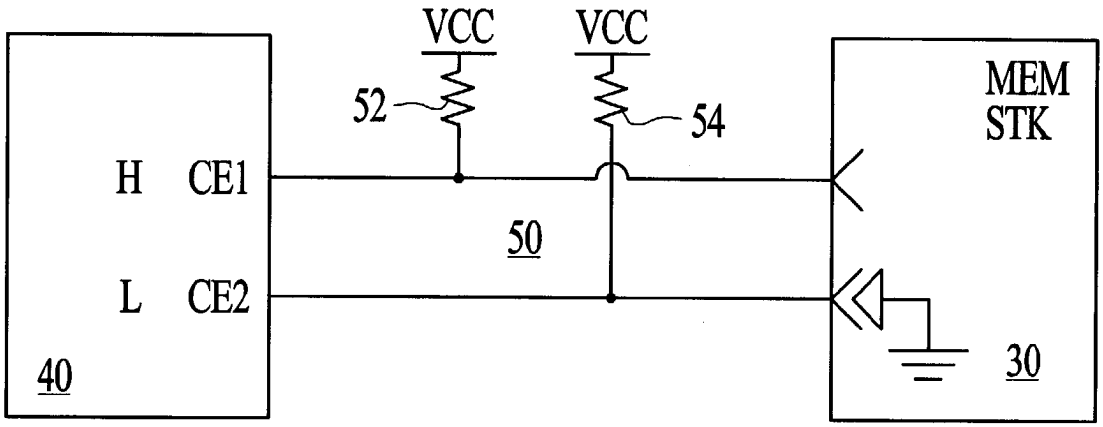

VCC
VCC
52
54
H CE1
50
H CE2
CF
16
40
44
HH = CF

FIG. 4B



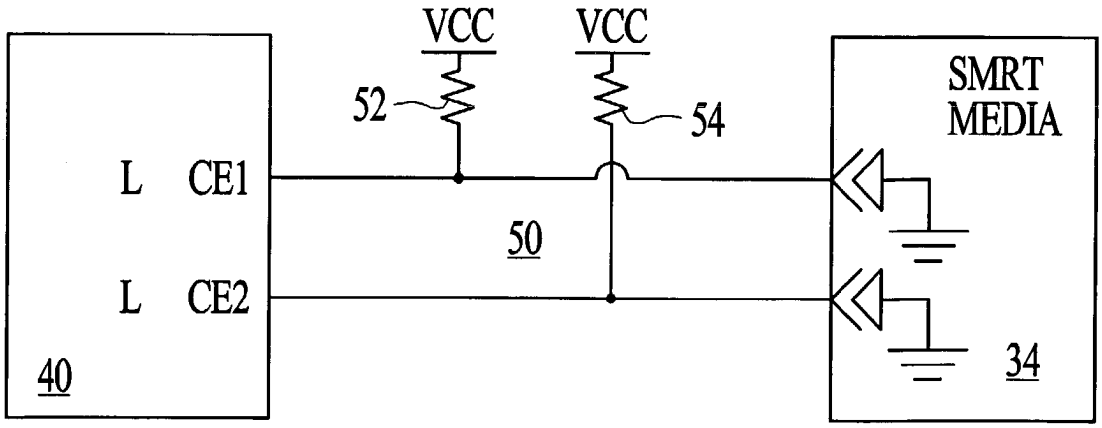
LH = MMC/SD

FIG. 4C



HL = MEM STK

FIG. 4D



LL = SMRT MEDIA

FIG. 4E

Pin	CF	Smart Media	MMC/SD	Memory Stick
1	Ground	Ground	Ground	Ground
2	D3	D3	—	—
3	D4	D4	—	—
4	D5	D5	—	—
5	D6	D6	—	—
6	D7	D7	—	—
7	-CE1	-SMCS	—	—
8	A10	—	—	—
9	-OE	-OE	—	—
10	A9	—	—	—
11	A8	—	—	—
12	A7	—	—	—
13	Power	Power	Power	Power
14	A6	CLE		
15	A5	ALE		
16	A4	READY		
17	A3	-WP		
18	A2	LVD	SCLK	SCLK
19	A1		DIO	DIO
20	A0		CMD	BS
21	D0	D0		
22	D1	D1		
23	D2	D2		
24	—	—	—	—
25	-CD2	-CD2	-CD2	-CD2
26	-CD1	-CD1	-CD1	-CD1
27	D11	—	—	—
28	D12	—	—	—
29	D13	—	—	—
30	D14	—	—	—
31	D15	—	—	—
32	-CE2	—	—	—
33	—	—	—	—
34	tie high	—	—	—
35	tie high	—	—	—
36	-WE	-WE	—	—
37	INTRQ	—	—	—
38	Power	Power	Power	Power
39	—	—	—	—
40	—	—	—	—
41	RESET	—	—	—
42	—	—	—	—
43	—	—	—	—
44	-REG	—	—	—
45	—	—	—	—
46	—	—	—	—
47	D8	—	—	—
48	D9	—	—	—
49	D10	—	—	—
50	Ground	Ground	Ground	Ground

FIG. 5

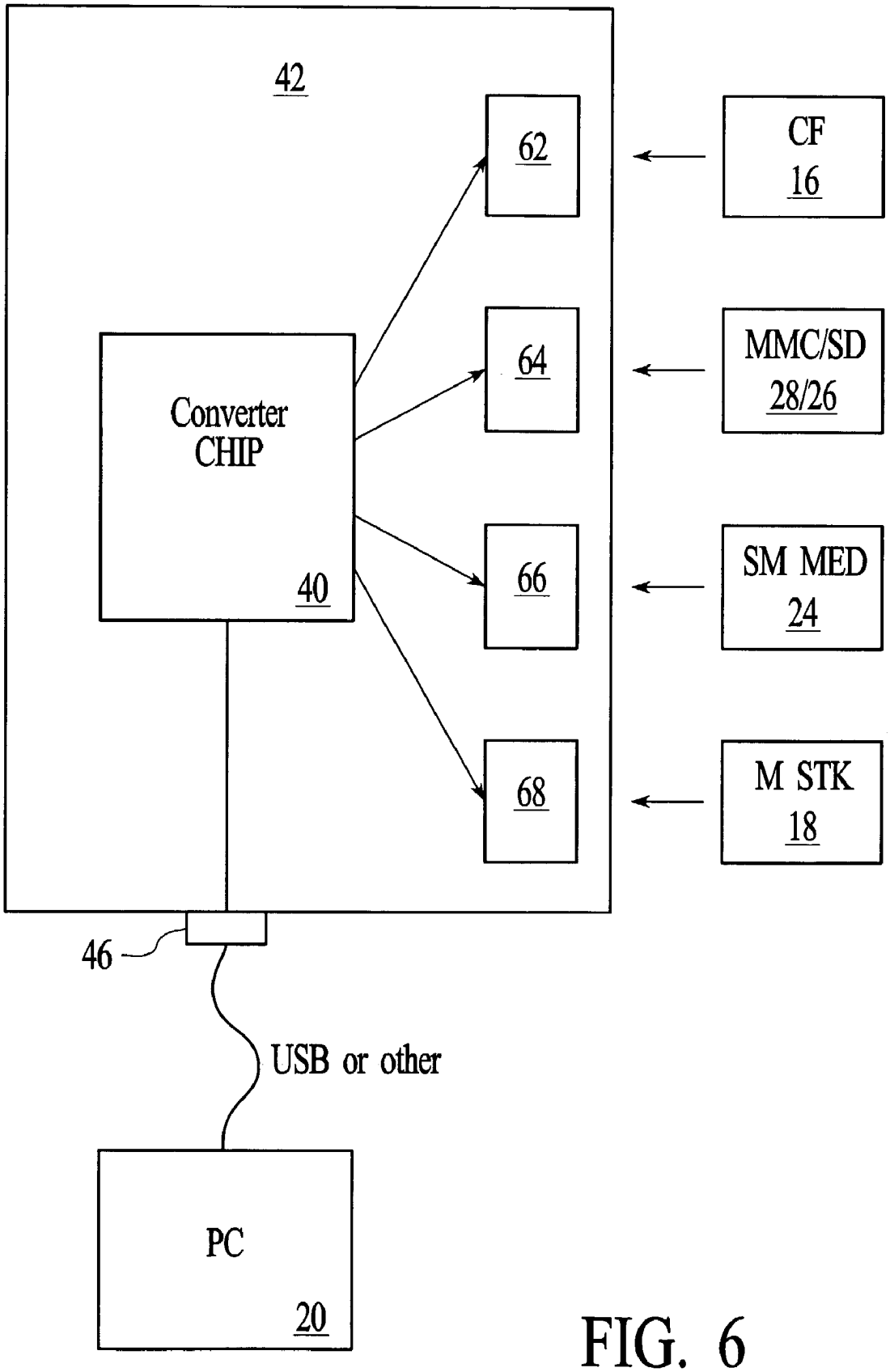

42
62
64
66
68
CF
16
MMC/SD
28/26
SM MED
24
M STK
18
Converter
CHIP
40
46
USB or other
PC
20

FIG. 6

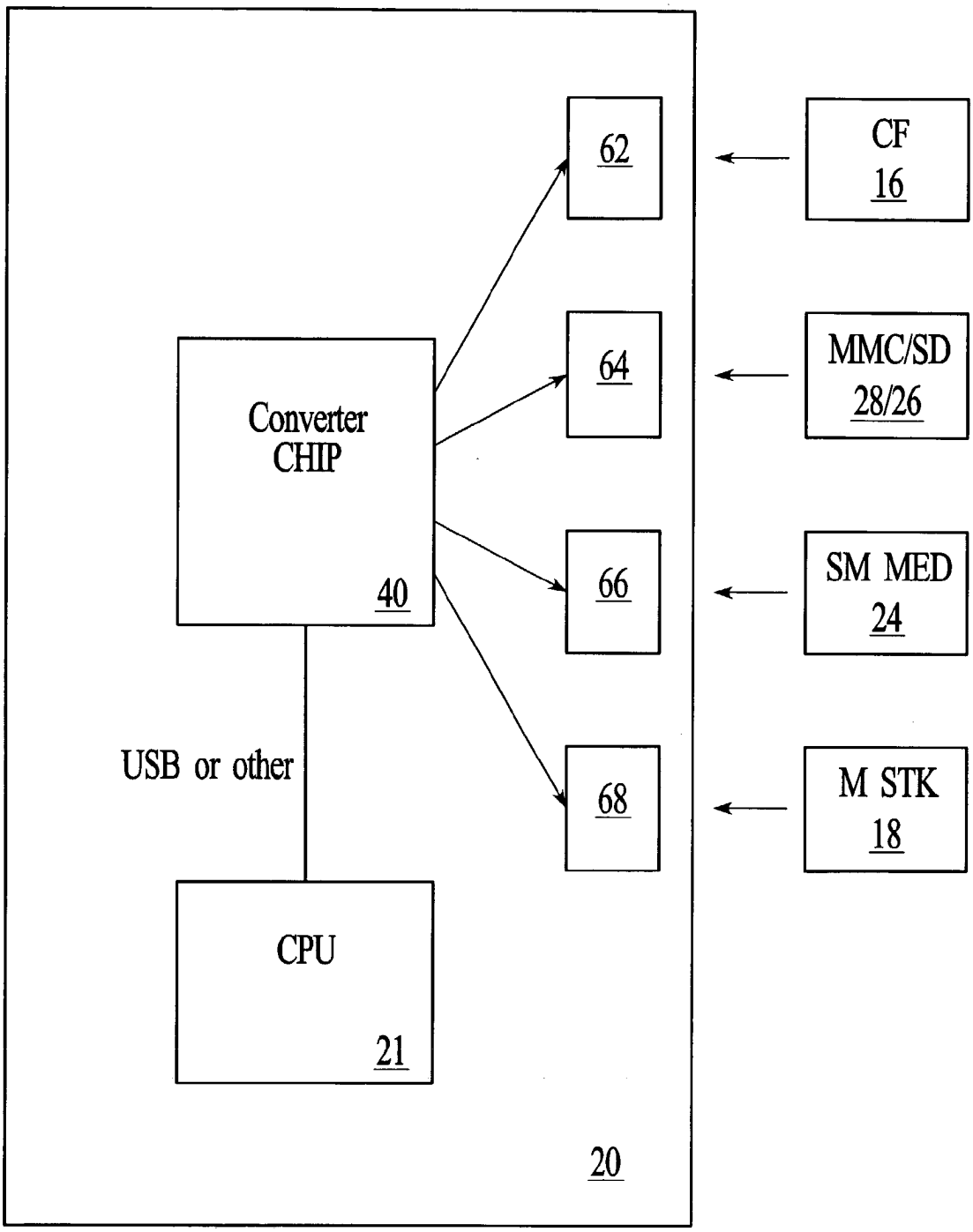

62
CF
16
64
MMC/SD
28/26
Converter
CHIP
40
66
SM MED
24
USB or other
68
M STK
18
CPU
21
20

FIG. 7

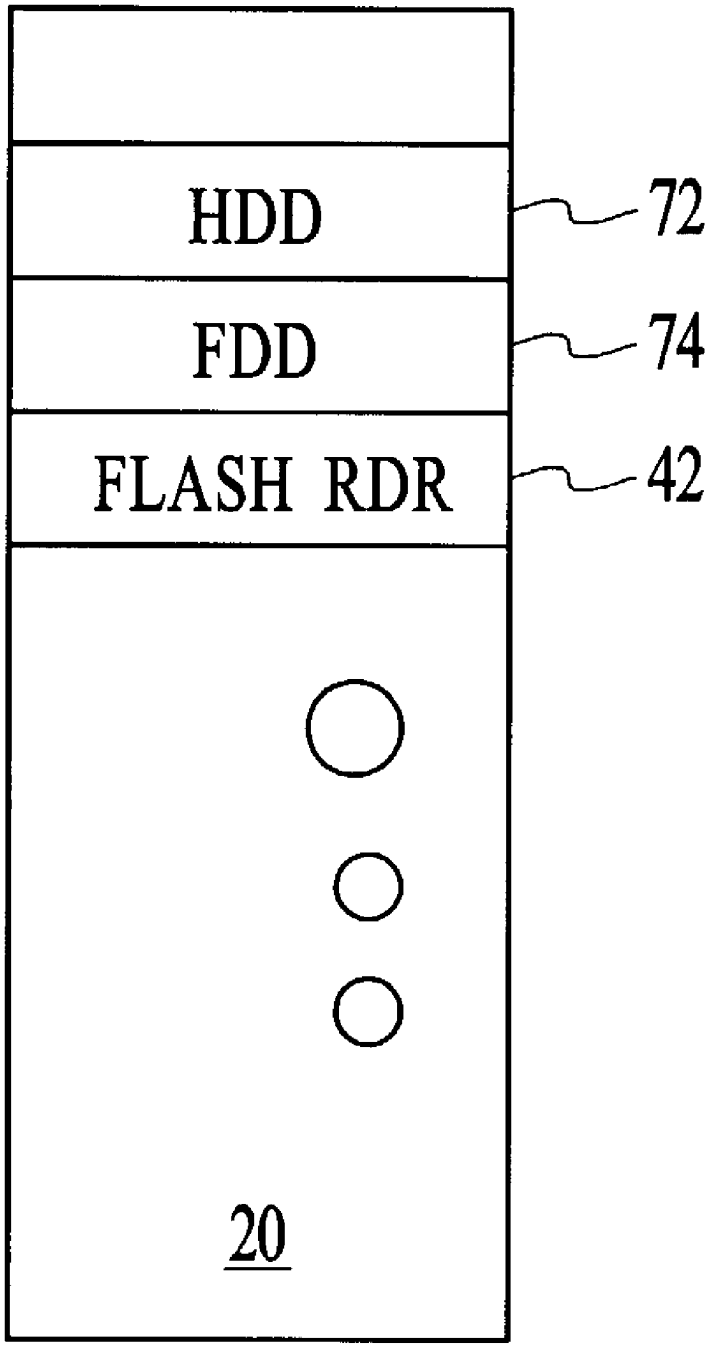


FIG. 8

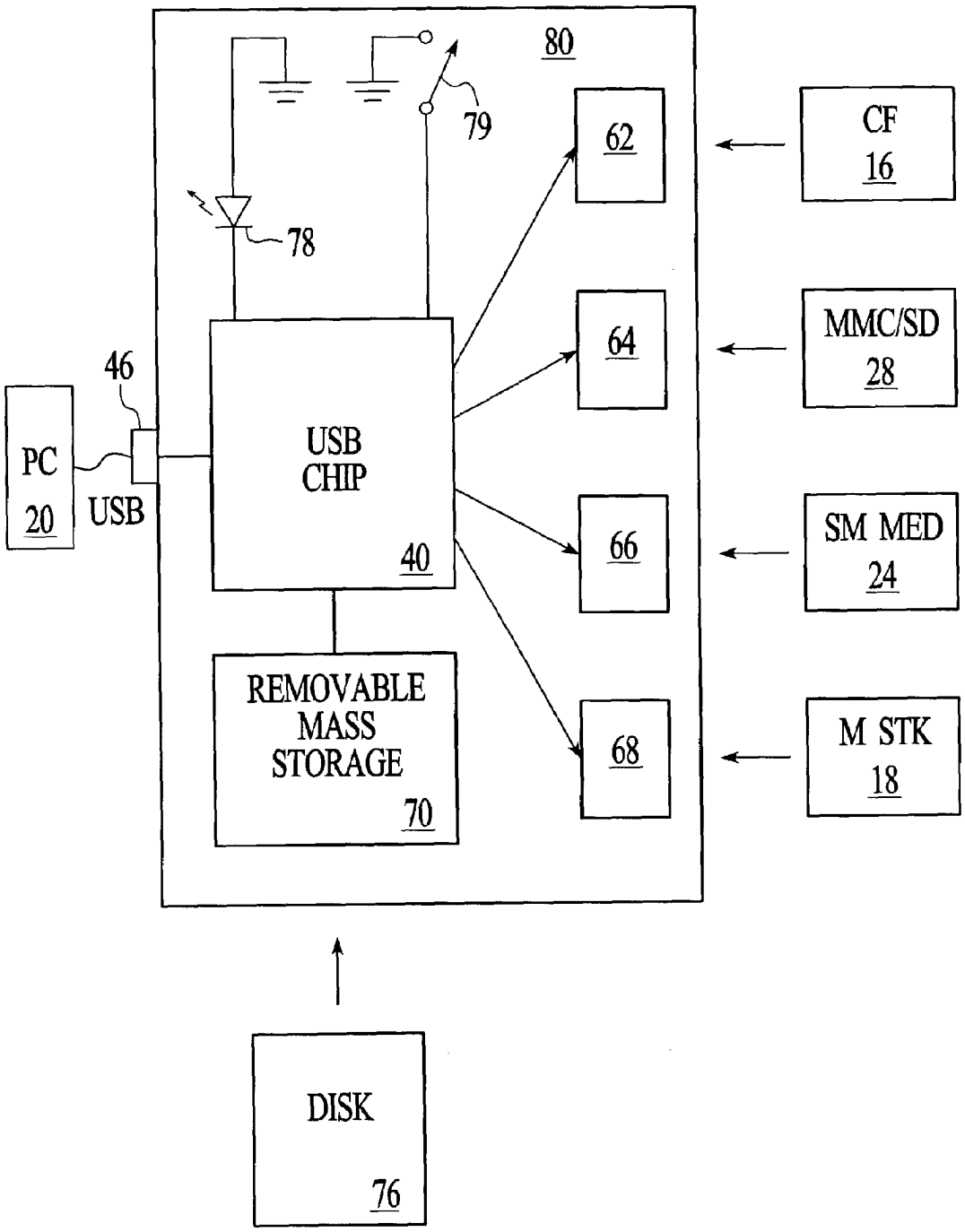

80
79
78
62
64
66
68
CF
16
MMC/SD
28
SM MED
24
M STK
18
46
PC
20
USB
USB
CHIP
40
REMOVABLE
MASS
STORAGE
70
DISK
76

FIG. 9

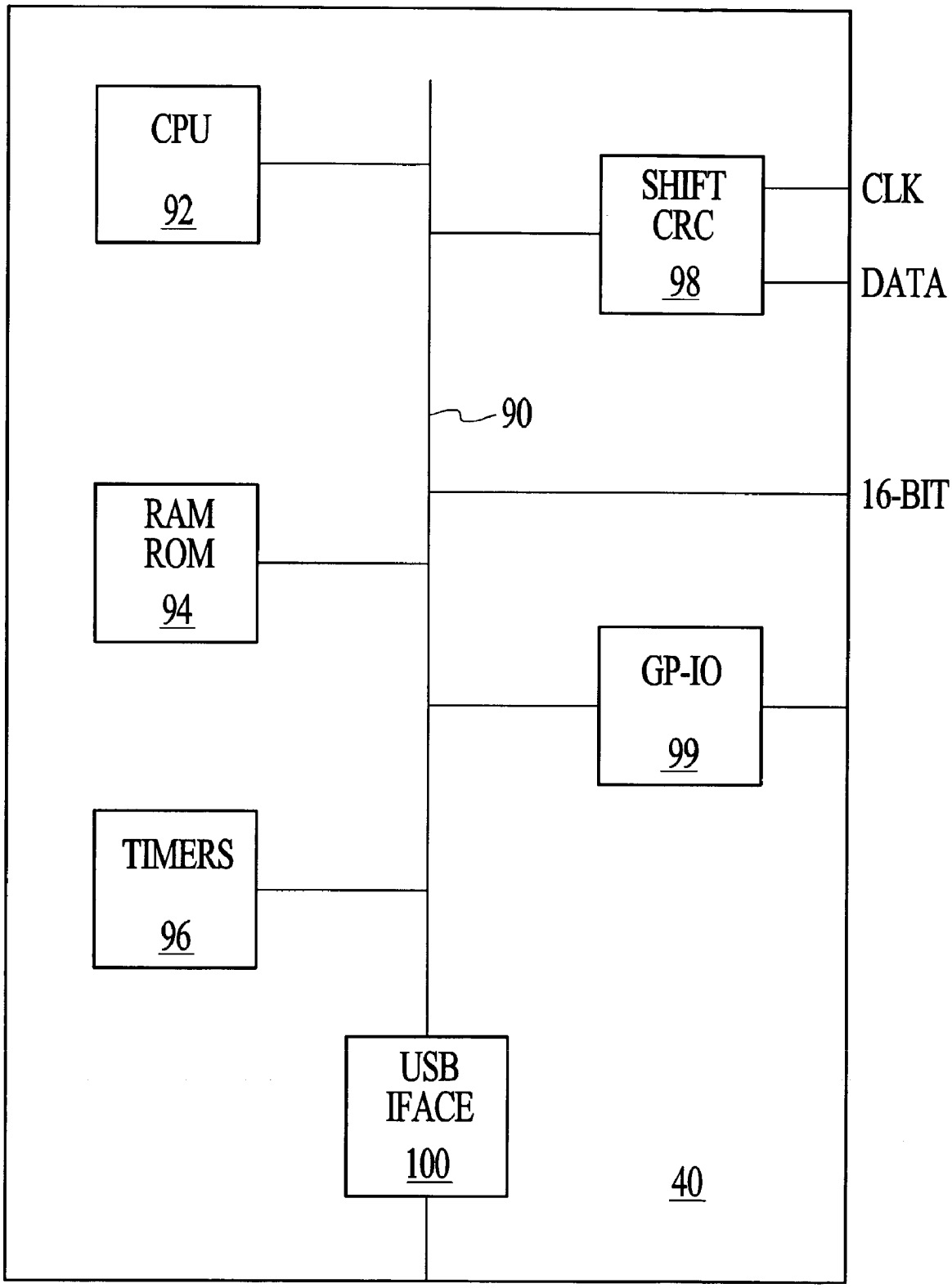

CPU
92
SHIFT
CRC
98
CLK
DATA
90
16-BIT
RAM
ROM
94
GP-IO
99
TIMERS
96
USB
IFACE
100
40

FIG. 10

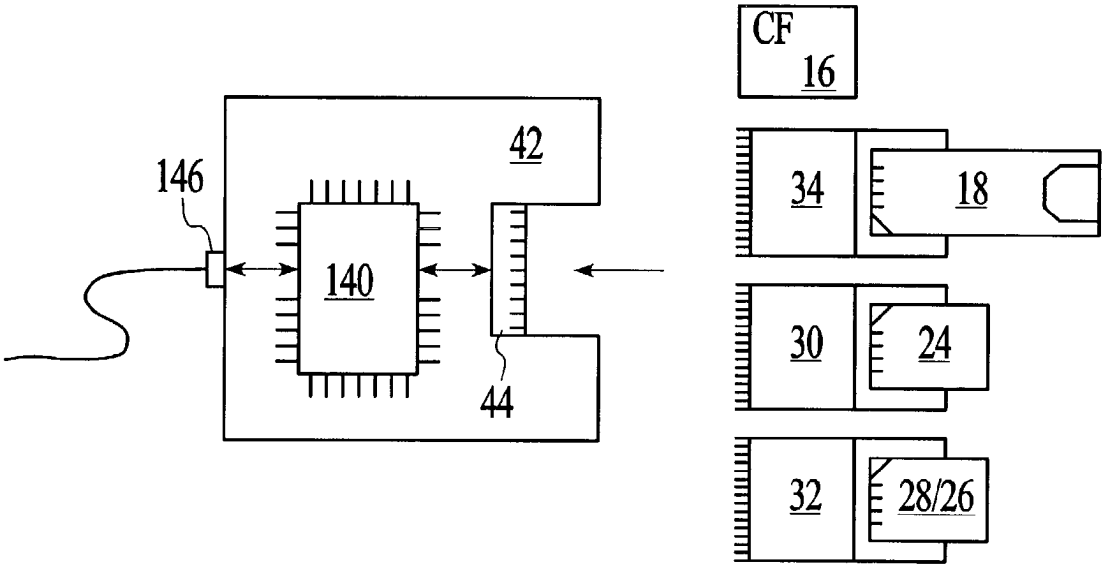


FIG. 11

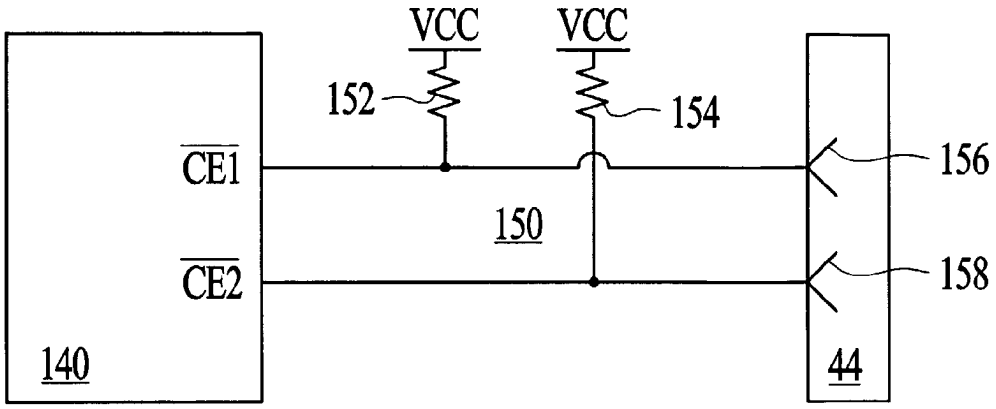


FIG. 12A

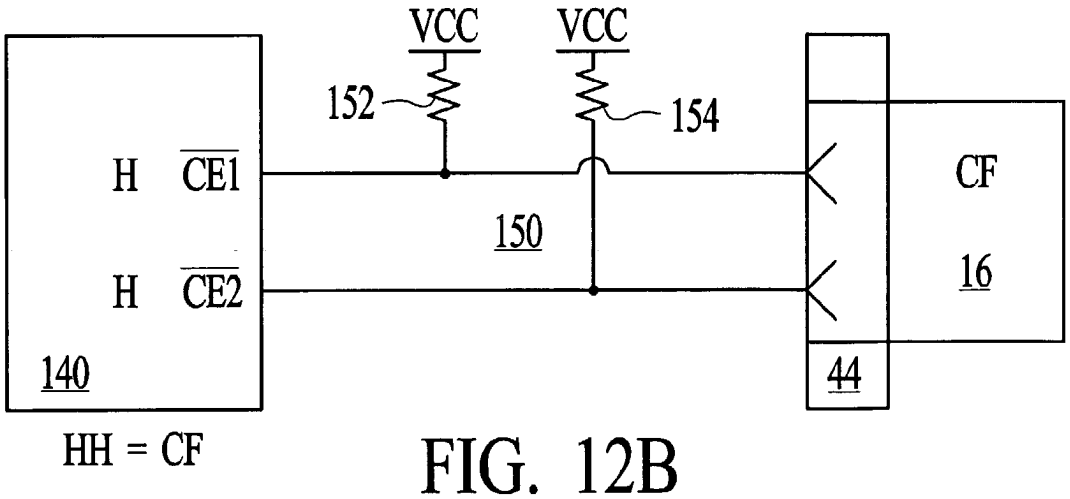
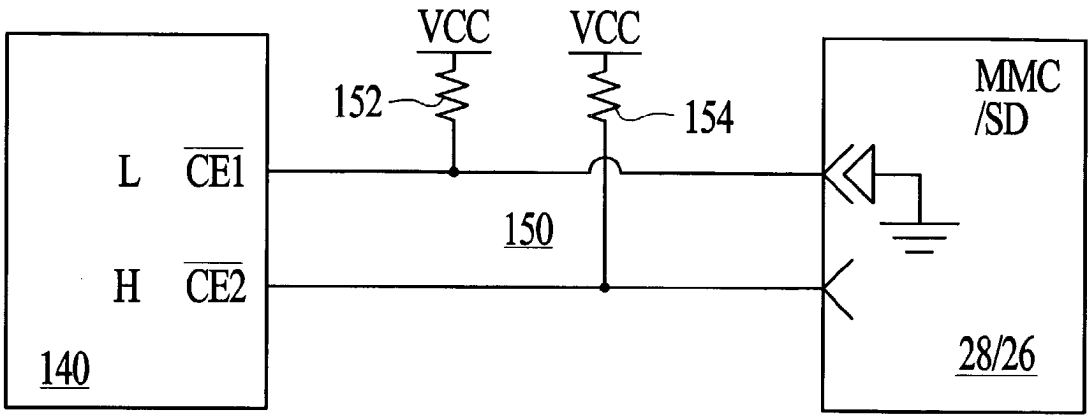
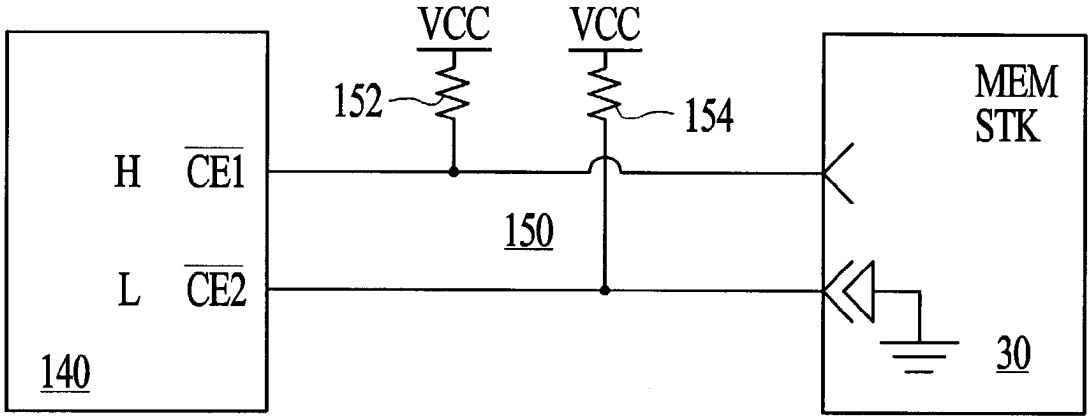


FIG. 12B



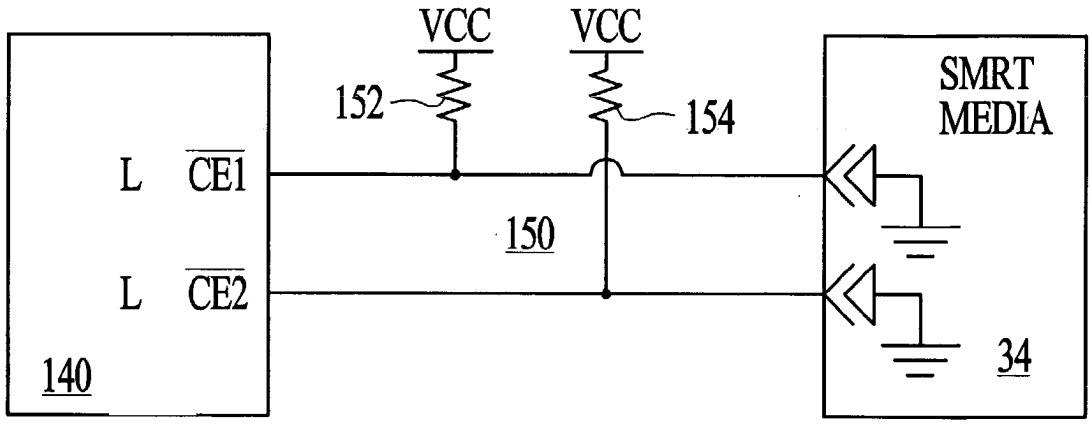
LH = MMC/SD

FIG. 12C



HL = MEM STK

FIG. 12D



LL = SMRT MEDIA

FIG. 12E

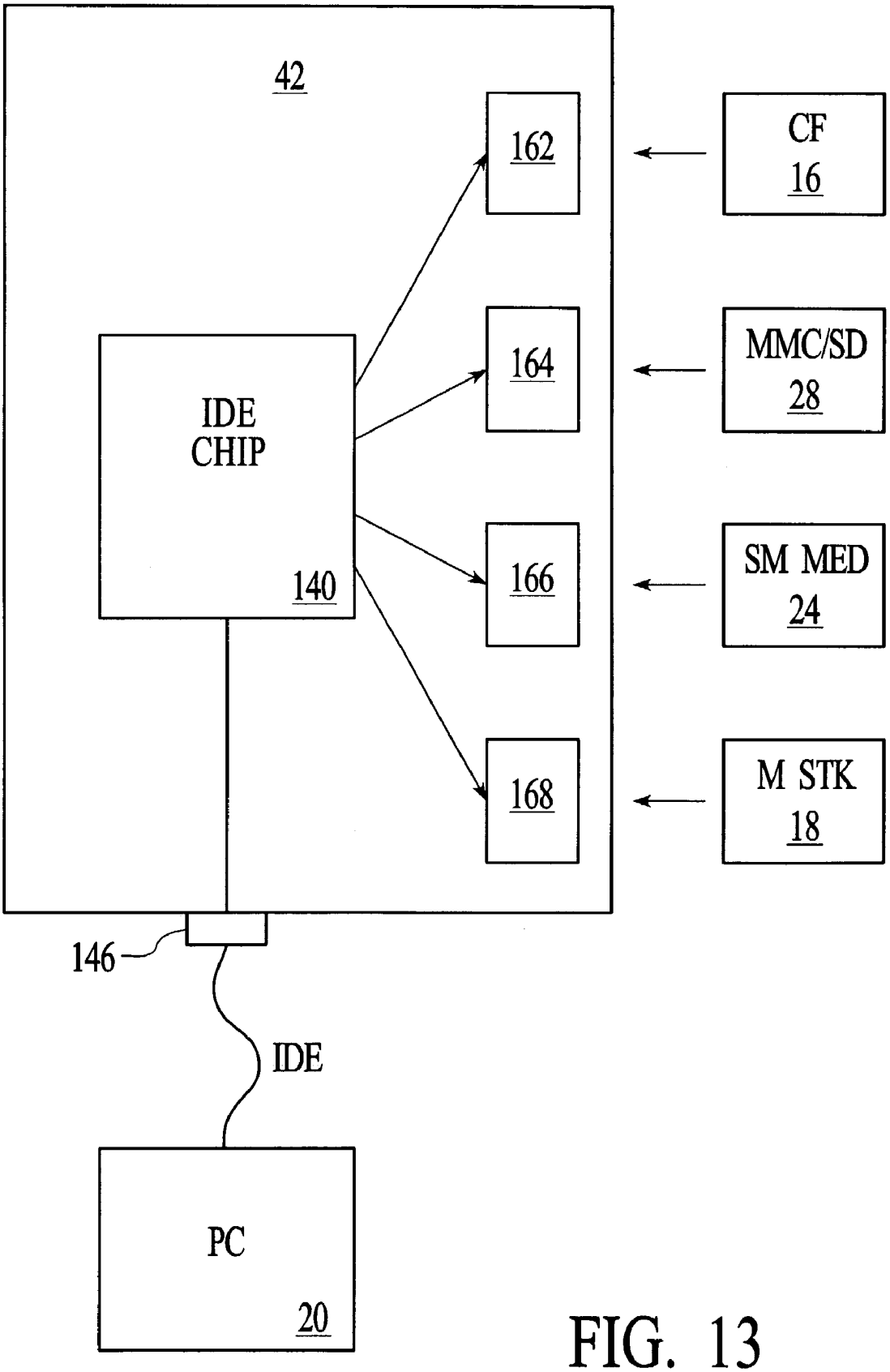

42
162
164
166
168
IDE
CHIP
140
CF
16
MMC/SD
28
SM MED
24
M STK
18
146
IDE
PC
20

FIG. 13

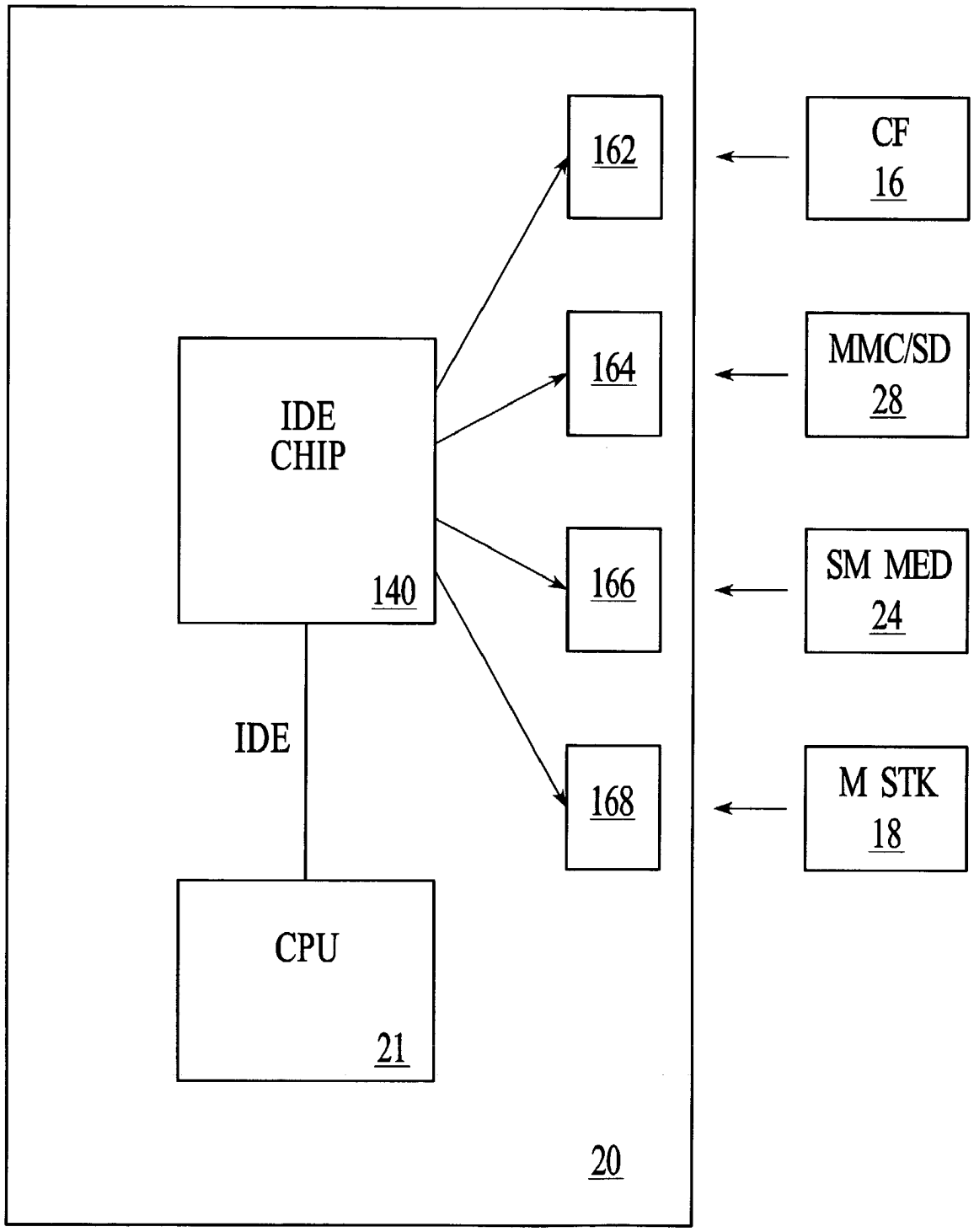

162
CF
16
164
MMC/SD
28
IDE
CHIP
140
166
SM MED
24
IDE
168
M STK
18
CPU
21
20

FIG. 14

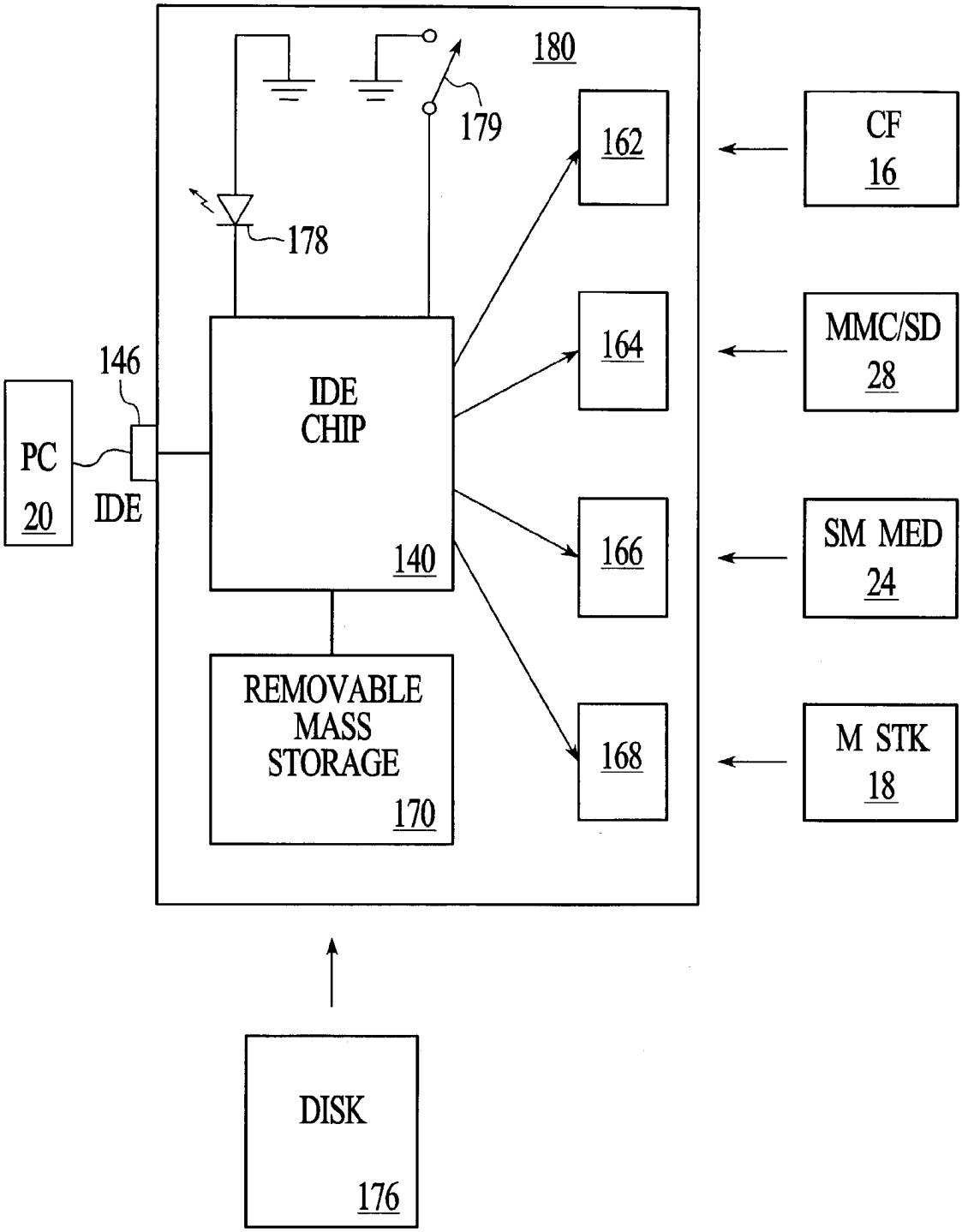

180
179
178
162
164
166
168
CF
16
MMC/SD
28
SM MED
24
M STK
18
146
PC
20
IDE
IDE
CHIP
140
REMOVABLE
MASS
STORAGE
170
DISK
176

FIG. 15

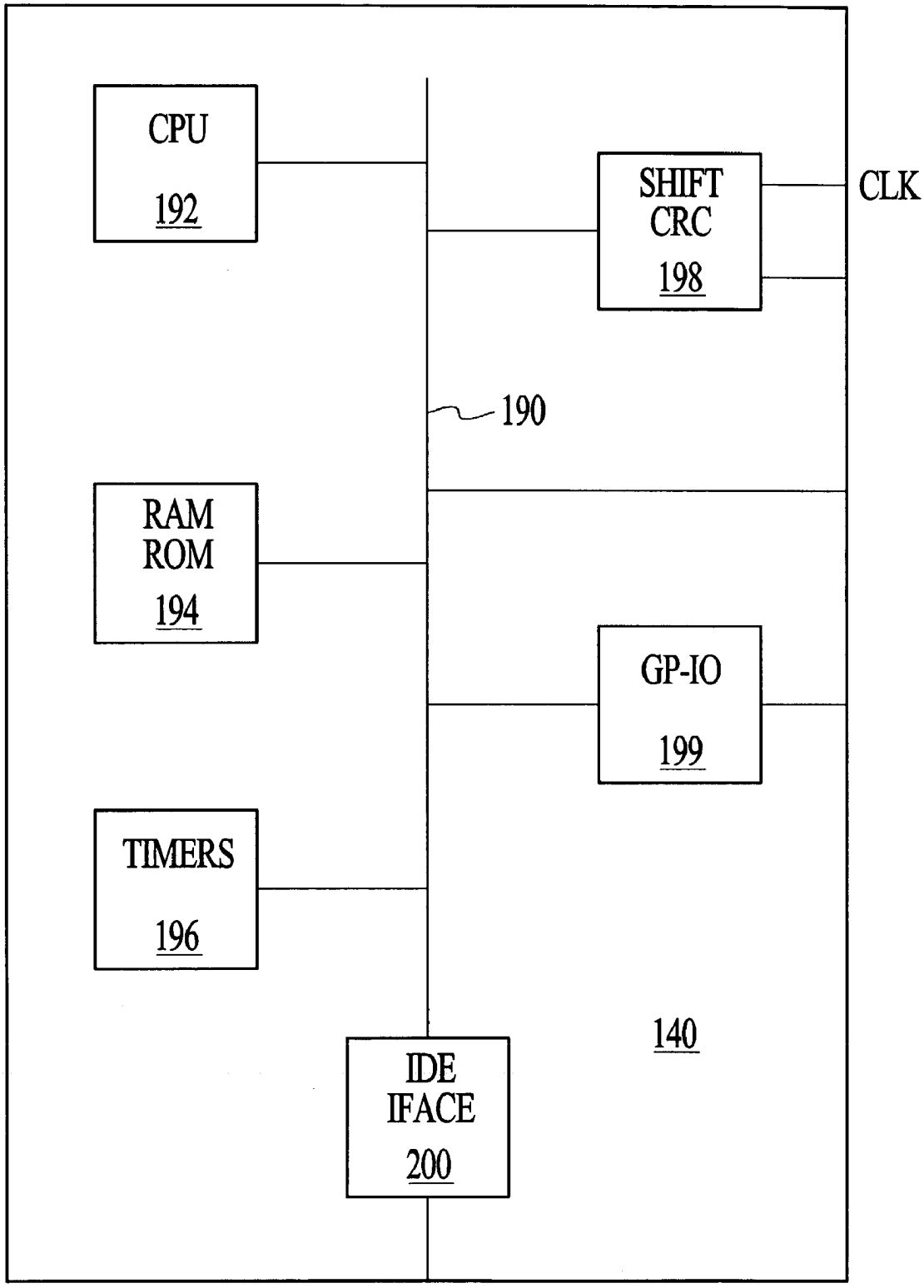

CPU
192
SHIFT
CRC
198
CLK
190
RAM
ROM
194
GP-IO
199
TIMERS
196
140
IDE
IFACE
200

FIG. 16

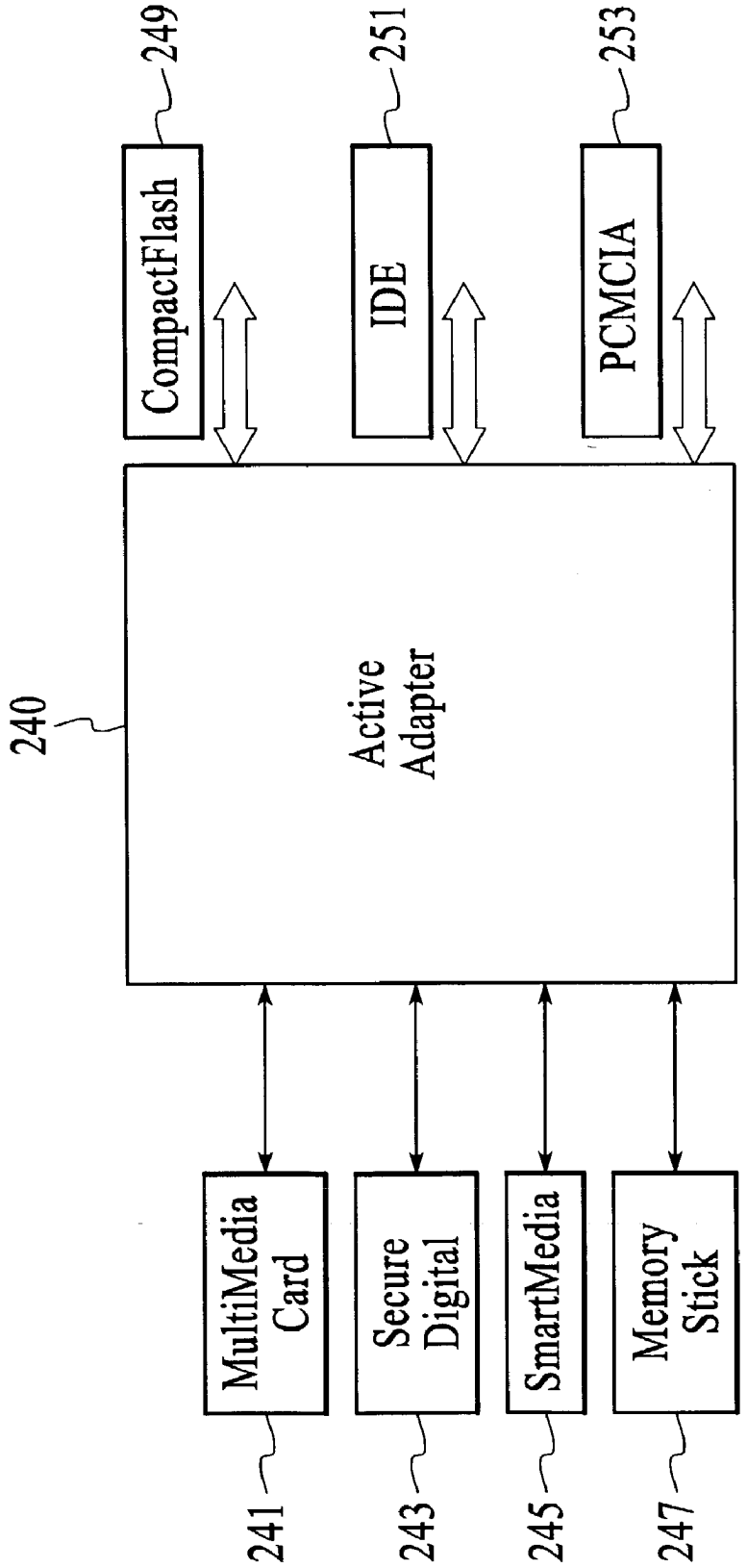

249
251
253
CompactFlash
IDE
PCMCIA
240
Active Adapter
242
MultiMedia Card
Secure Digital
SmartMedia
Memory Stick
241
243
245
247

FIG. 17

Sl. No	Flash adapter (Input)	Interface (Output)
1	MultiMediaCard (MMC)	CompactFlash
2	MultiMediaCard (MMC)	IDE
3	MultiMediaCard (MMC)	PCMCIA
4	Secure Digital Card (SD)	CompactFlash
5	Secure Digital Card (SD)	IDE
6	Secure Digital Card (SD)	PCMCIA
7	SmartMedia (SM)	CompactFlash
8	SmartMedia (SM)	IDE
9	SmartMedia (SM)	PCMCIA
10	Memory Stick (MS)	CompactFlash
11	Memory Stick (MS)	IDE
12	Memory Stick (MS)	PCMCIA
13	CompactFlash (CF)	IDE
14	CF + SM + MS + MMC + SD	IDE
15	CF Console with adapters for SM, MS, MMC, SD	IDE

FIG. 18

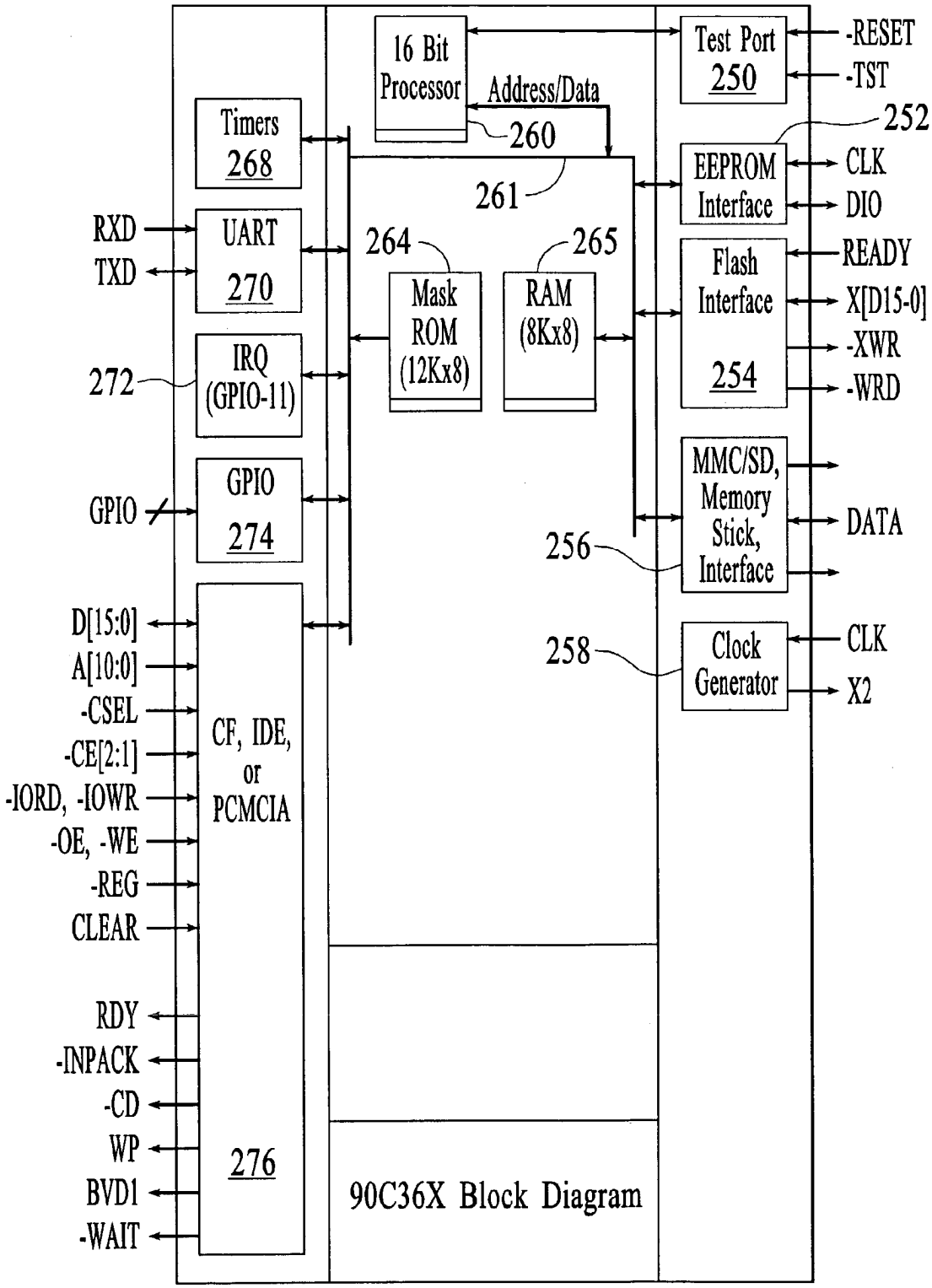

16 Bit Processor
Address/Data
260
261
Test Port 250
-RESET
-TST
252
Timers 268
EEPROM Interface
CLK
DIO
RXD
TXD
UART 270
264
265
Mask ROM (12Kx8)
RAM (8Kx8)
Flash Interface 254
READY
X[D15-0]
-XWR
-WRD
272
IRQ (GPIO-11)
GPIO
GPIO 274
MMC/SD, Memory Stick, Interface
DATA
256
D[15:0]
A[10:0]
-CSEL
-CE[2:1]
-IORD, -IOWR
-OE, -WE
-REG
CLEAR
258
Clock Generator
CLK
X2
CF, IDE, or PCMCIA
RDY
-INPACK
-CD
WP
BVD1
-WAIT
276
90C36X Block Diagram

FIG. 19

Pin	CF	Smart Media	MMC/SD	Memory Stick
1	Ground	Ground	Ground	Ground
2	D3	D3	—	—
3	D4	D4	—	—
4	D5	D5	—	—
5	D6	D6	—	—
6	D7	D7	—	—
7	-CE1	-SMCS	—	—
8	A10	—	—	—
9	-OE	-OE	—	—
10	A9	—	—	—
11	A8	—	—	—
12	A7	—	—	—
13	Power	Power	Power	Power
14	A6	CLE		
15	A5	ALE		
16	A4	READY		
17	A3	-WP		
18	A2	LVD	SERCLK	SERCLK
19	A1		DATAIO	DATAIO
20	A0		CMD	BITSET
21	D0	D0		
22	D1	D1		
23	D2	D2		
24	—	—	—	—
25	-CD2	-CD2	-CD2	-CD2
26	-CD1	-CD1	-CD1	-CD1
27	D11	—	—	—
28	D12	—	—	—
29	D13	—	—	—
30	D14	—	—	—
31	D15	—	—	—
32	-CE2	—	—	—
33	—	—	—	—
34	tie high	—	—	—
35	tie high	—	—	—
36	-WE	-WE	—	—
37	INTRQ	—	—	—
38	Power	Power	Power	Power
39	—	—	—	—
40	—	—	—	—
41	RESET	—	—	—
42	—	—	—	—
43	—	—	—	—
44	-REG	—	—	—
45	—	—	—	—
46	—	—	—	—
47	D8	—	—	—
48	D9	—	—	—
49	D10	—	—	—
50	Ground	Ground	Ground	Ground

FIG. 20

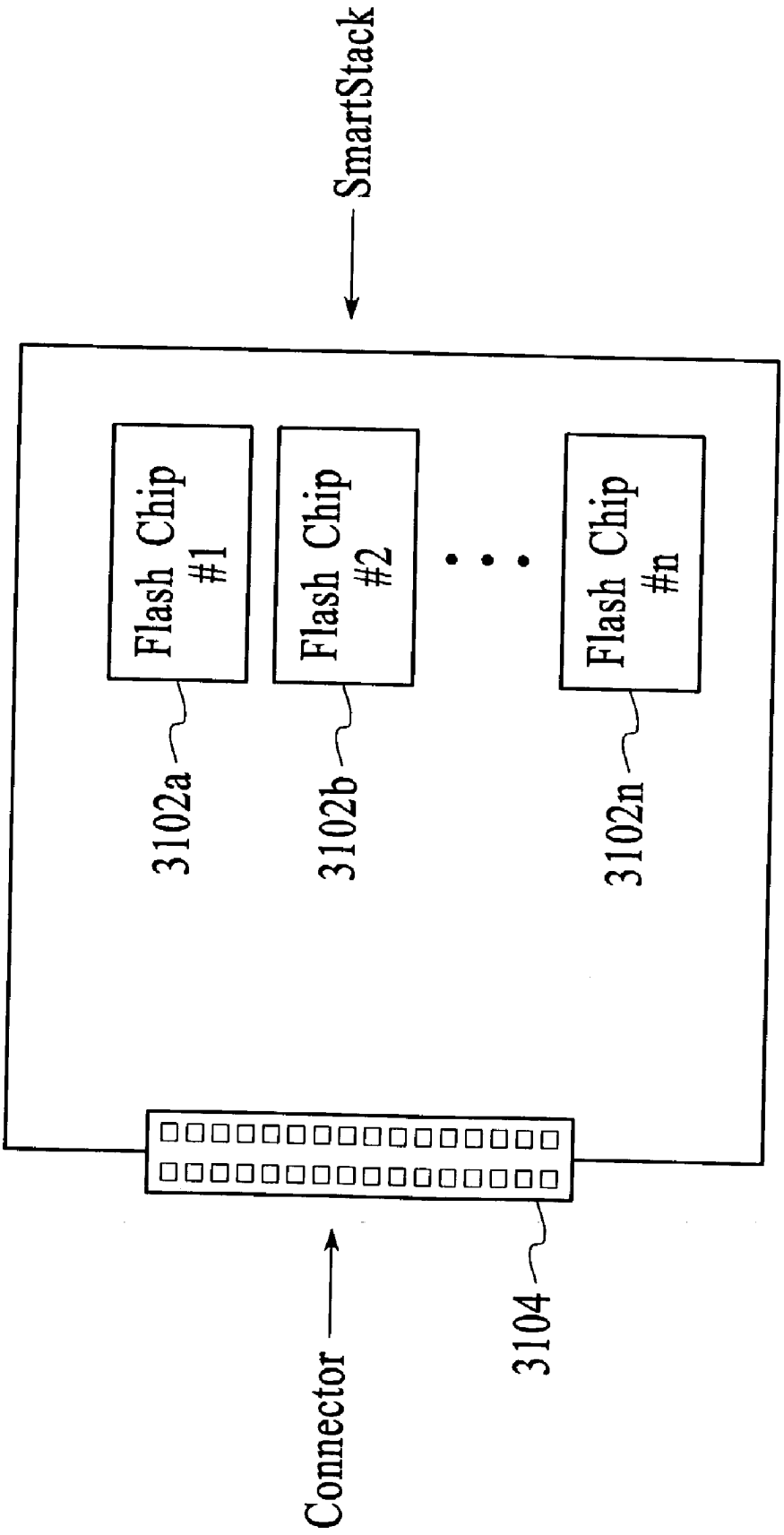

SmartStack
Flash Chip #1
Flash Chip #2
Flash Chip #n
3102a
3102b
3102n
3104
Connector

FIG. 21

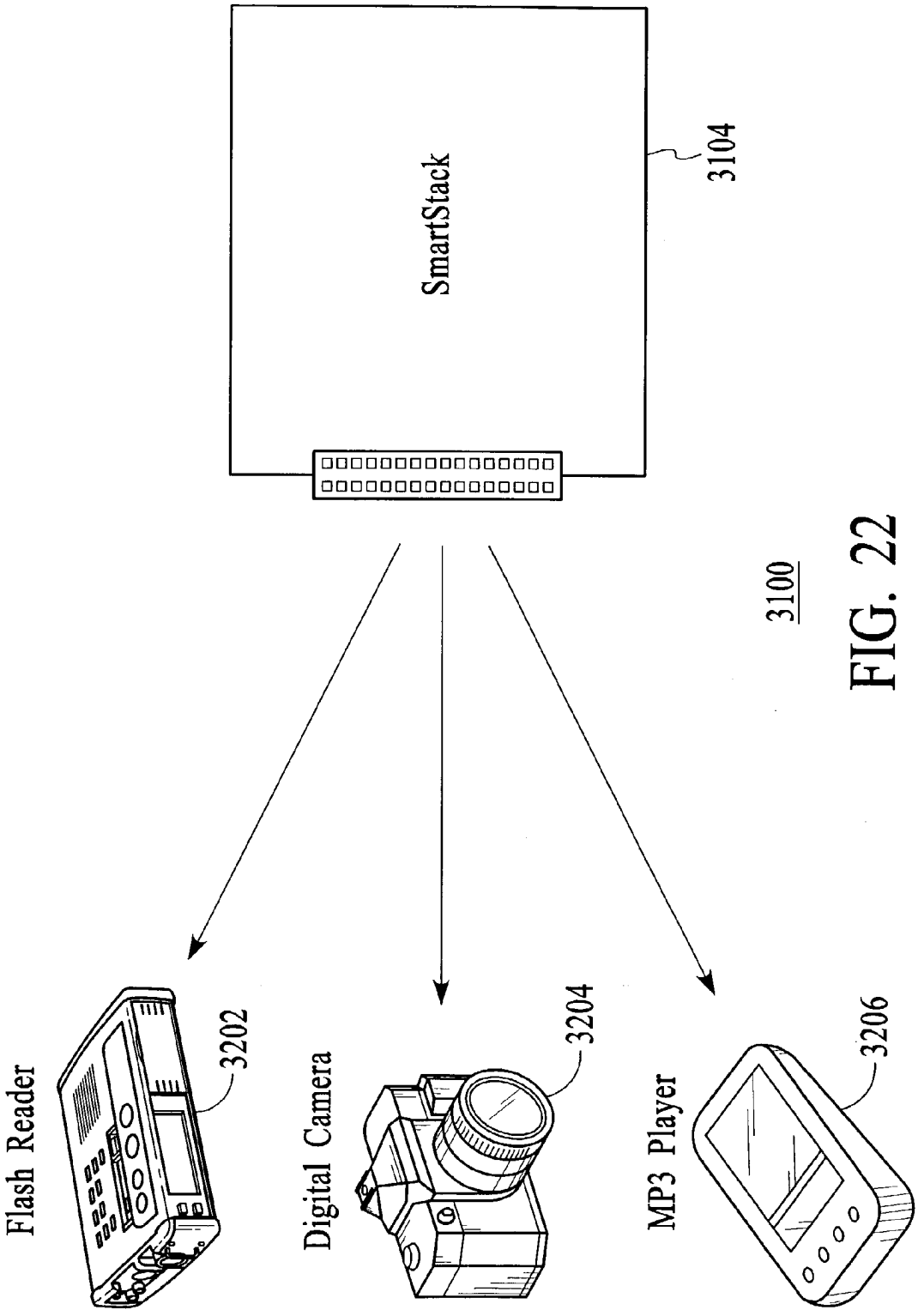

SmartStack
3104
3100
Flash Reader
3202
Digital Camera
3204
MP3 Player
3206

FIG. 22

Media Type	CE1	CE2	A3	A5	A6	CD1	CD2
CompactFlash	1	1	1	1	1	0	0
Memory Stick	1	0	1	1	1	0	0
MMC/SD card	0	1	1	1	1	0	X
SmartStack NAND	0	0	0	0	0	0	0
SmartStack NOR	0	0	1	0	0	0	0
Reserved	0	0	0	1	0	0	0
Reserved	0	0	1	1	0	0	0
Reserved	0	0	0	0	1	0	0
Reserved	0	0	1	0	1	0	0
Reserved	0	0	0	1	1	0	0
Smart Media	0	0	1	1	1	0	0

FIG. 23

S[3:0]	Flash Chip
0	1
1	2
2	3
3	4
4	5
5	6
6	7
7	8
8	9
9	10
A	11
B	12

FIG. 24

Pin	CompactFlash Signal	SmartStack Signal
14	A6	S0
7	-CE1	S1
32	-CE2	S2
20	A0	S3

FIG. 24A

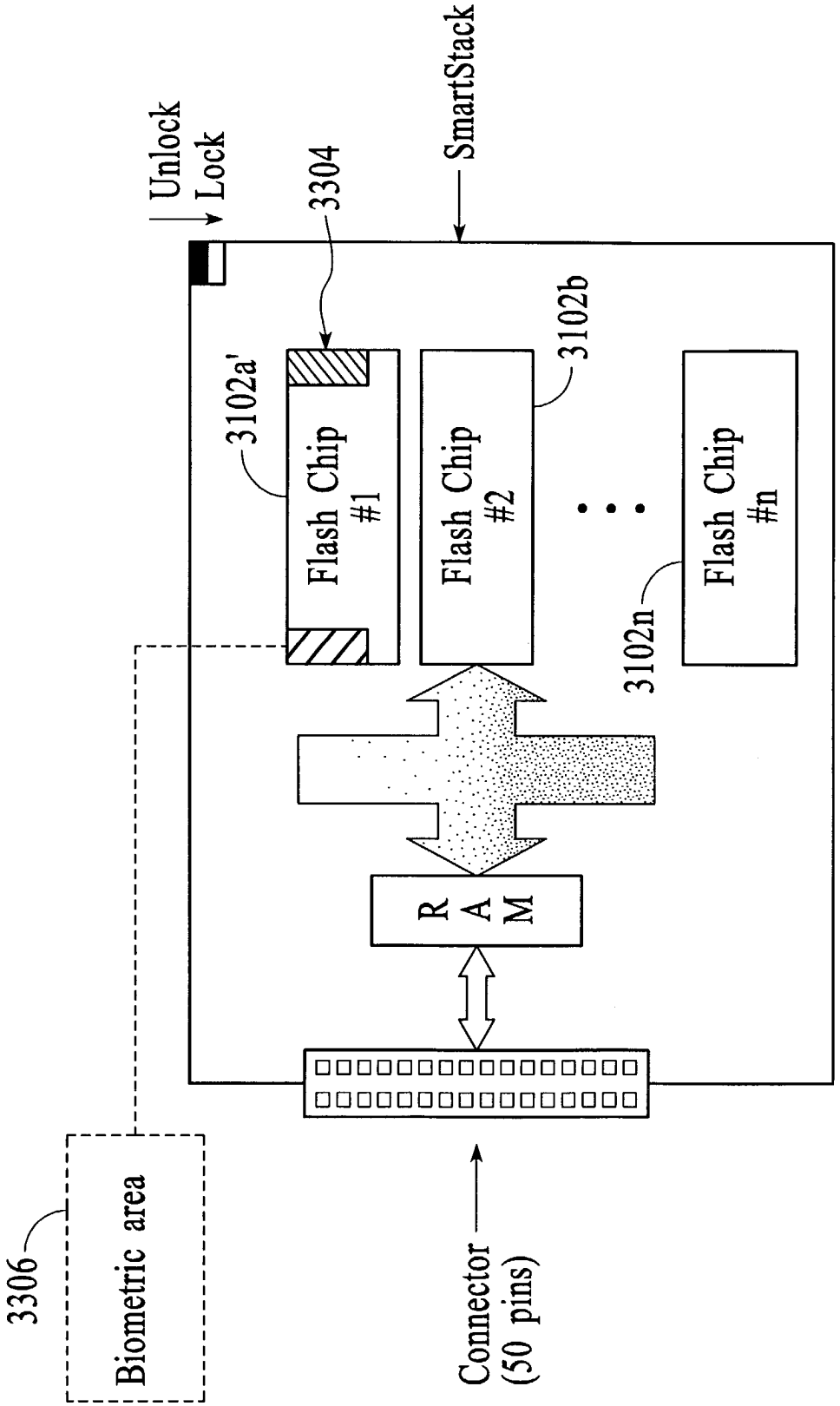

Unlock
Lock
3304
SmartStack
3102a'
Flash Chip #1
Flash Chip #2
3102b
Flash Chip #n
3102n
3300
R A M
3306
Biometric area
Connector (50 pins)

FIG. 25

Byte 0	Byte 1	Byte 2	Byte 3	Description
C3	B6	00	Xx	Reserved
C3	B6	01	AAH	Secure area starts here. If Byte 3 is AA, this is the last block, else it is 00 to denote a continuation in the next block.
C3	B6	02	AAH	Secure area ends here.
C3	B6	03	AAH	Biometric area starts here. If Byte 3 is AA, this is the last block, else it is 00.
C3	B6	04	AAH	Biometric area ends here.
C3	B6	05-54H	Xx	Reserved
C3	B6	55H	Xx	Start of Firmware block, fw is < 16K. If Byte 3 is 00, then there are more blocks to follow.
C3	B6	56H-A9H	Xx	Reserved
C3	B6	AAH	AAH	End of Firmware block. Byte 3 is AA to denote end block.
C3	B6	ABH-FEH	Xx	Reserved
C3	B6	FFH	FF	Blank block

FIG. 26

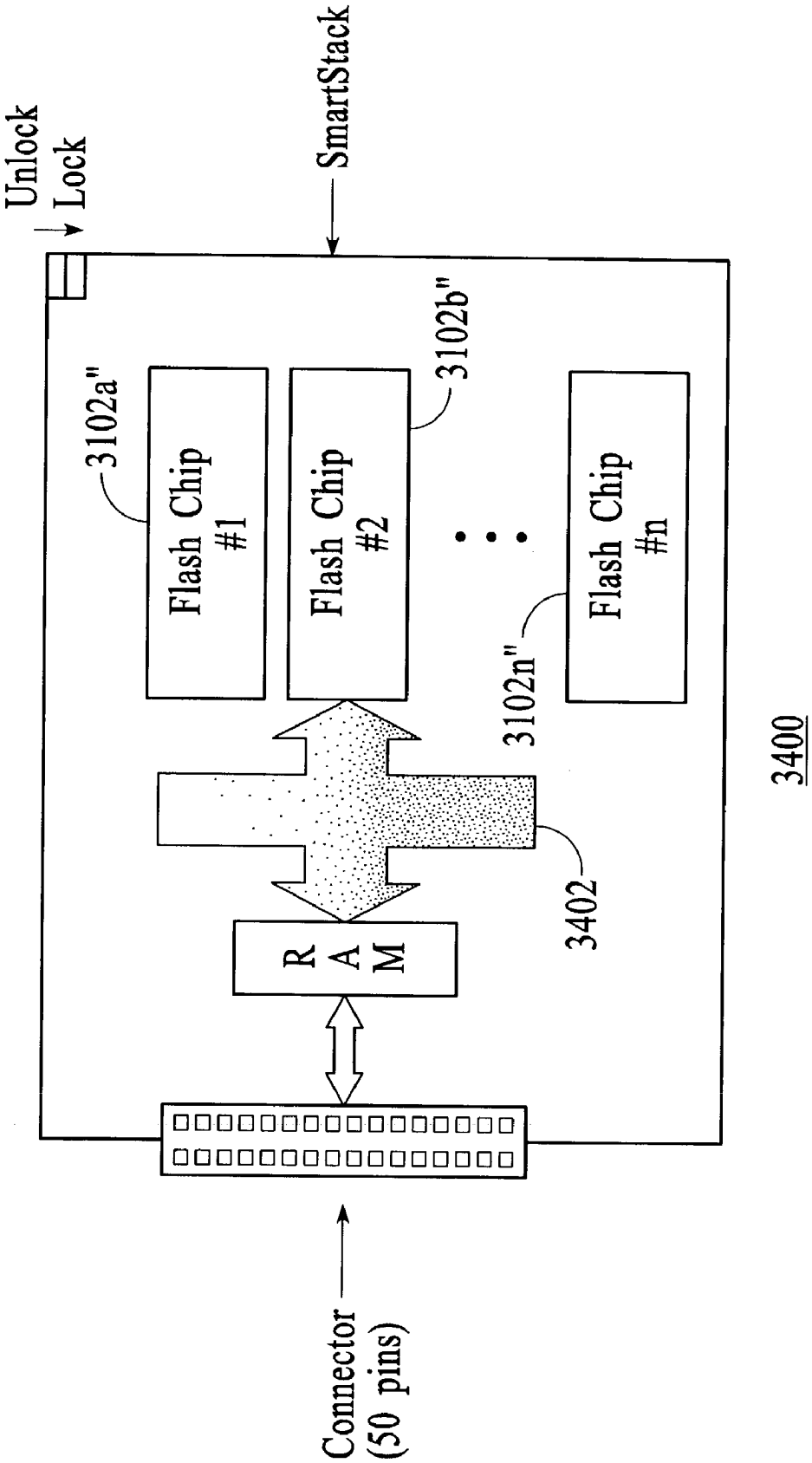

Unlock
Lock
SmartStack
3102a"
Flash Chip #1
Flash Chip #2
3102b"
Flash Chip #n
3102n"
3400
3402
R A M
Connector (50 pins)

FIG. 27

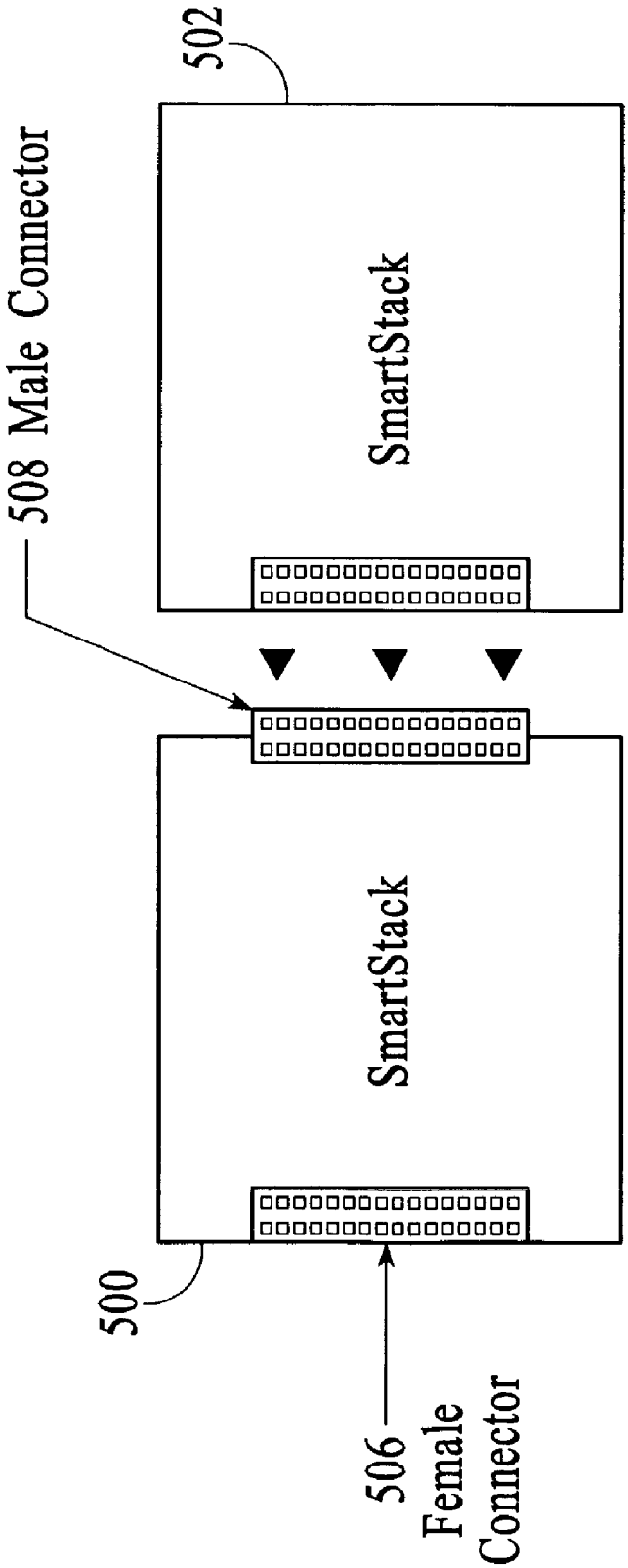
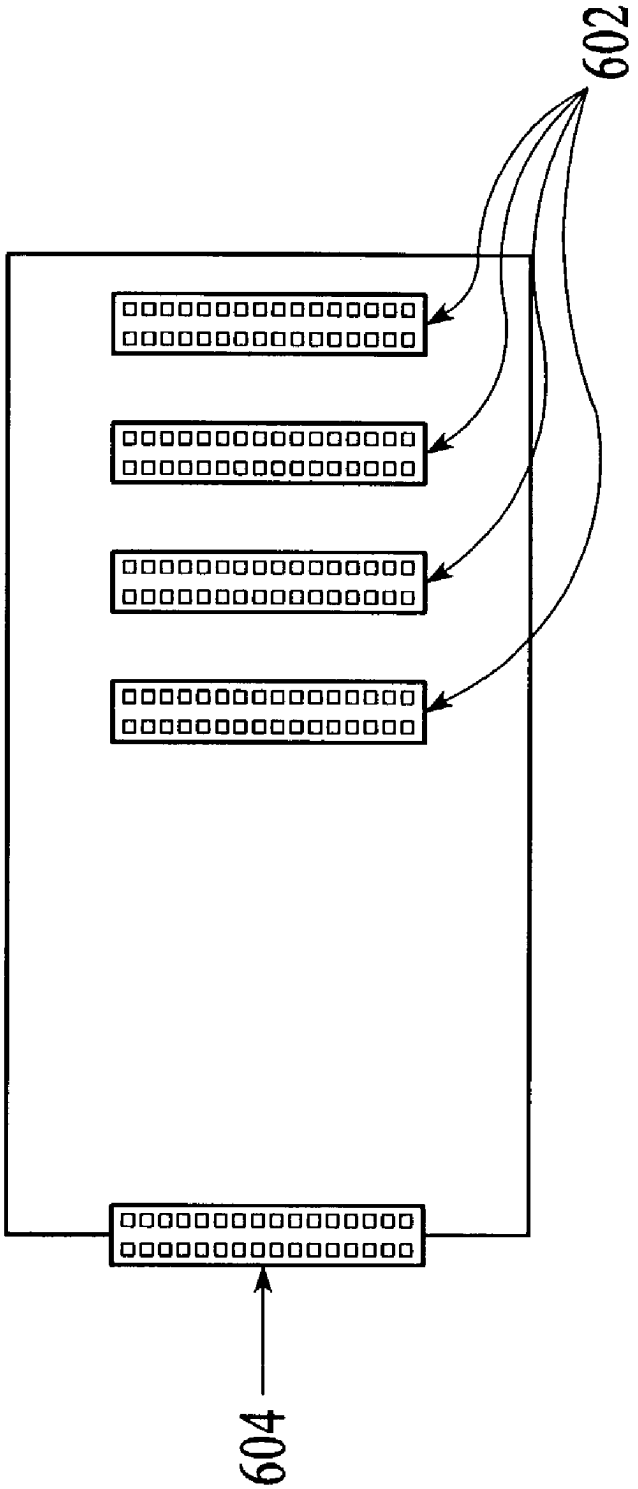

502
508 Male Connector
SmartStack
SmartStack
500
506
Female
Connector

FIG. 28



600

FIG. 29

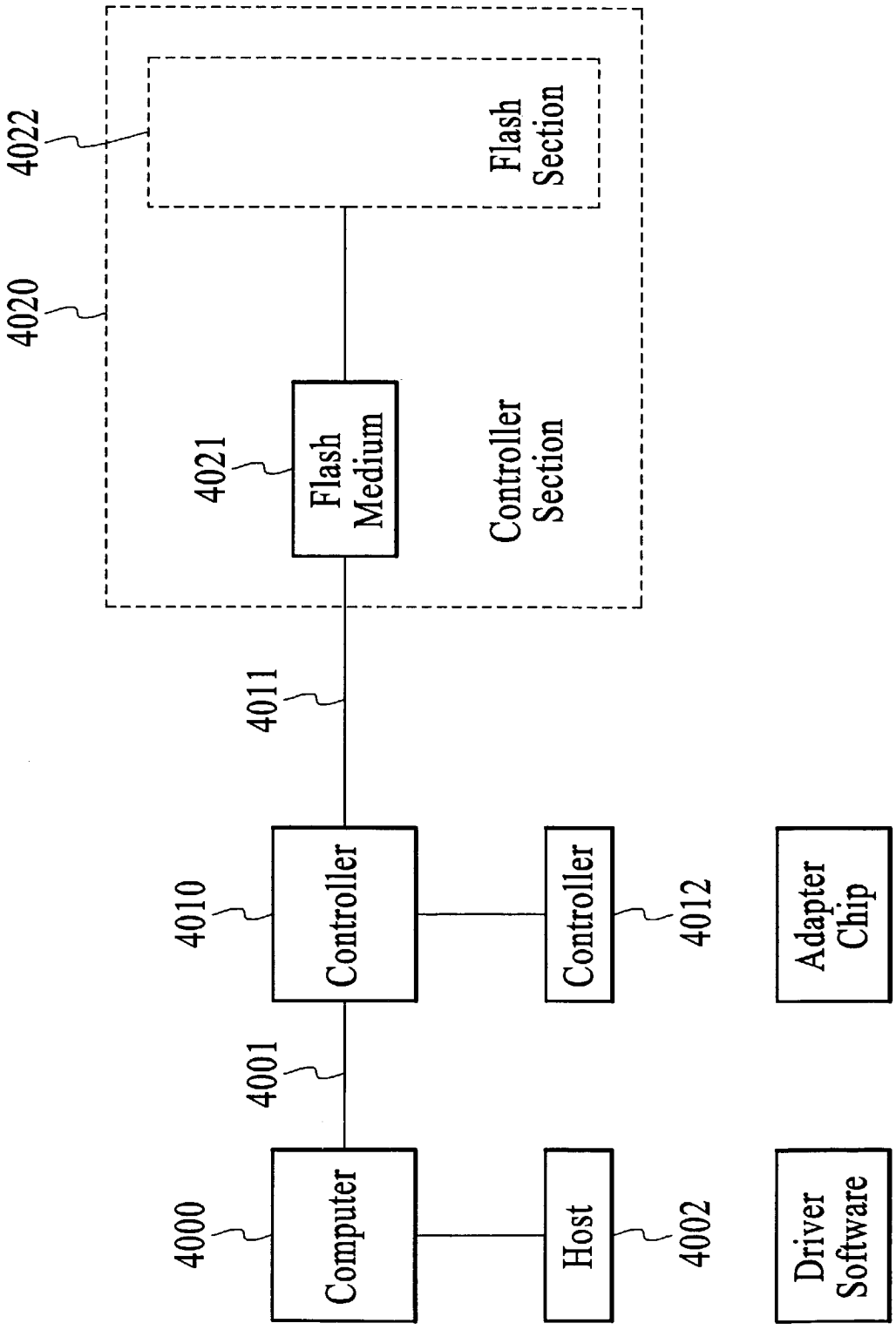

4022
Flash Section
4020
4021
Flash Medium
Controller Section
4011
4010
Controller
Controller
4012
Adapter Chip
4001
4000
Computer
Host
4002
Driver Software

FIG. 30

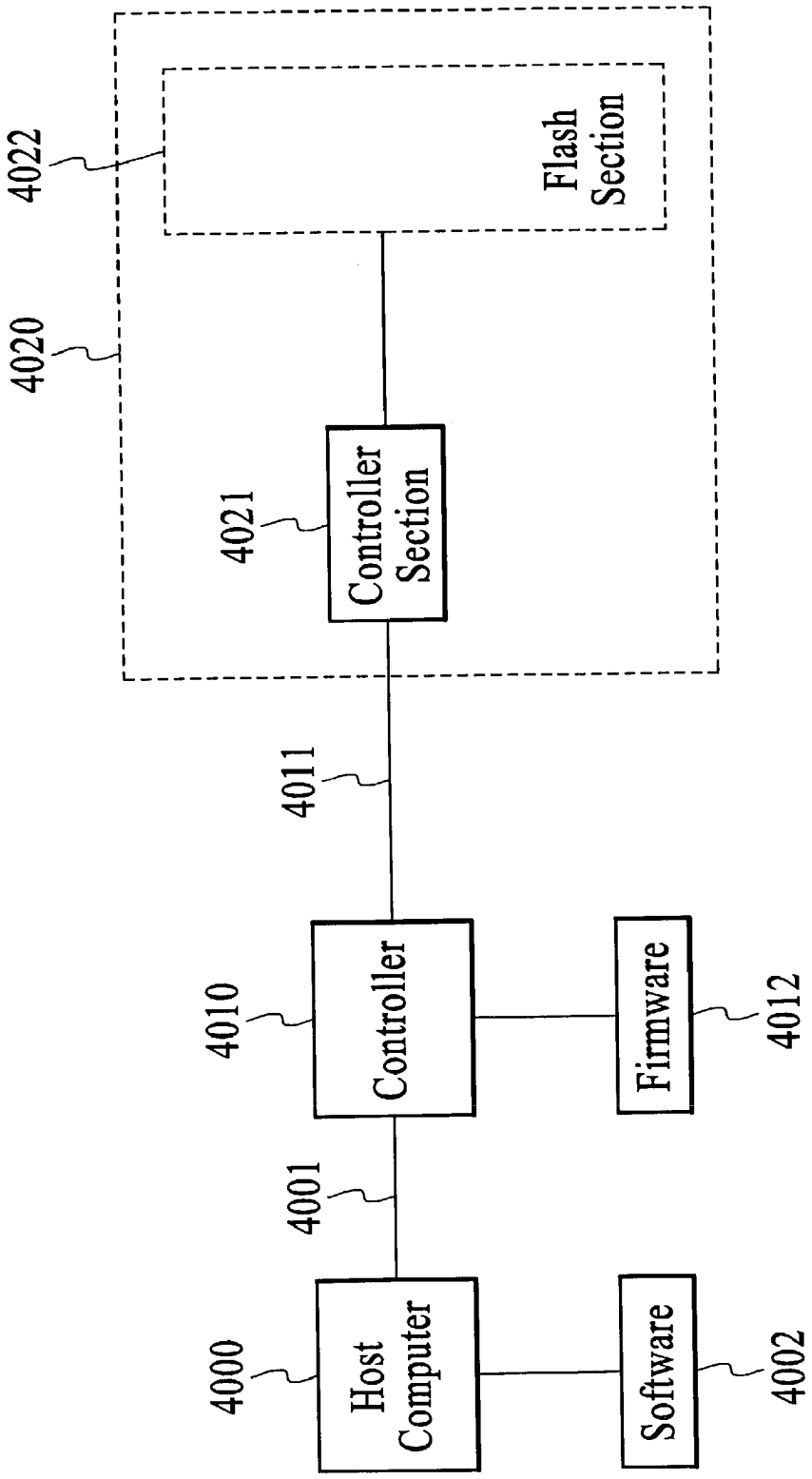

4022
Flash Section
4020
4021
Controller Section
4011
4010
Controller
Firmware
4012
4001
4000
Host Computer
Software
4002

FIG. 31

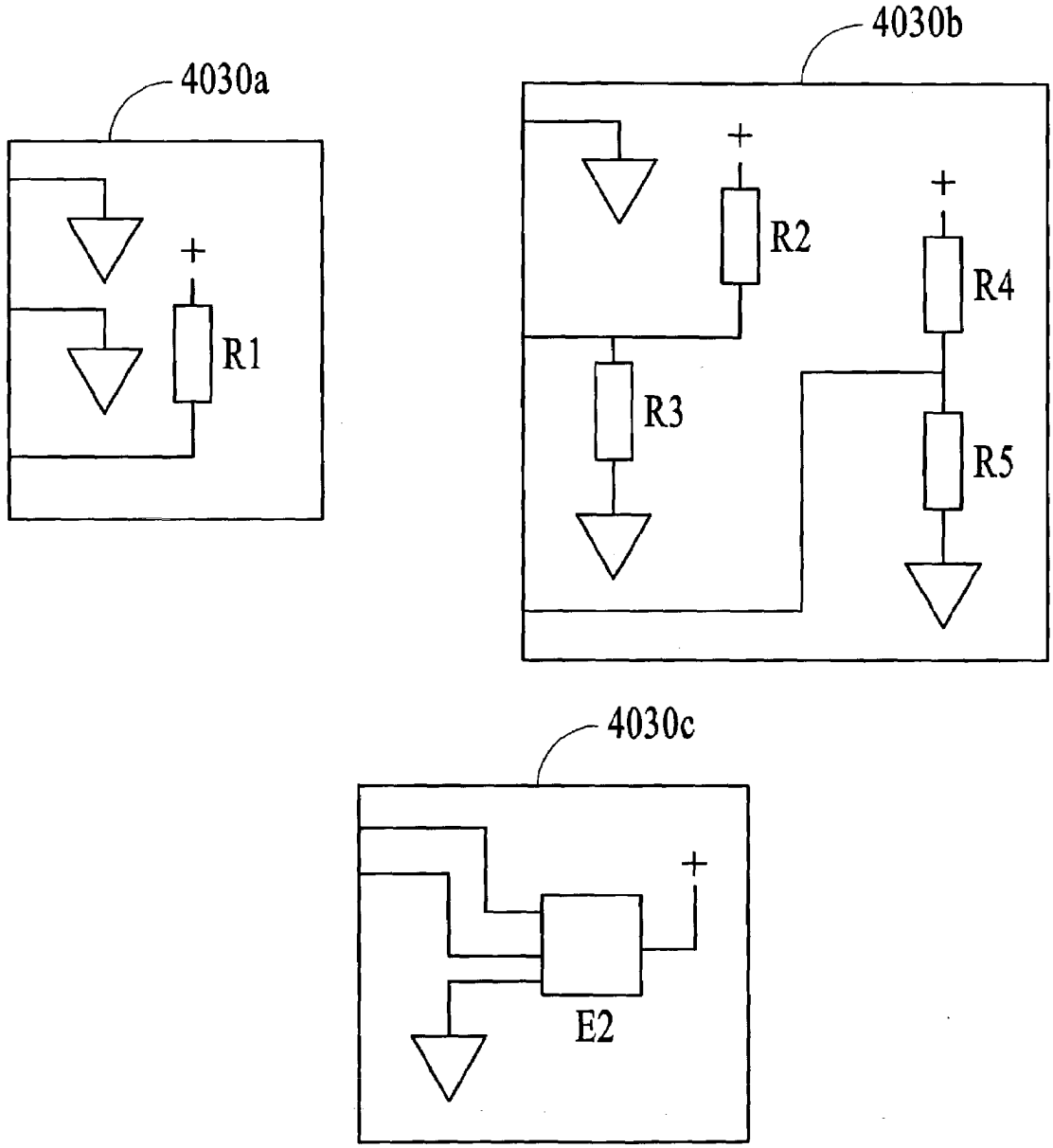


FIG. 32

MULTIMODE CONTROLLER FOR INTELLIGENT AND "DUMB" FLASH CARDS

RELATED APPLICATIONS

This application is claiming, under 35 USC §119(e), the benefit of provisional patent application Ser. No. 60/386,396 filed on Jun. 4, 2002.

Further, the present application is a continuation-in-part of applications Ser. No. 10/039,685, filed Oct. 29, 2001 now U.S. Pat. No. 6,832,281, entitled "Flashtoaster for Reading Several Types of Flash Memory Cards With or Without a PC," Ser. No. 10/002,567 filed Nov. 1, 2001 now abandoned, entitled "Active Adapter Chip for Use in a Flash Card Reader, and Ser. No. 10/063,021 filed Mar. 12, 2002, entitled "Memory Module Which Includes a Form Factor Connector."

FIELD OF THE INVENTION

The present invention relates generally to controllers and more particularly to controllers for Flash cards.

BACKGROUND OF THE INVENTION

Digital cameras have become one of the most popular of electronic devices. In a recent year, more digital cameras were sold than traditional film cameras. Images from digital cameras can be downloaded and stored on personal computers. Digital pictures can be converted to common formats such as JPEG and sent as e-mail attachments or posted to virtual photo albums on the Internet. Video as well as still images can be captured, depending on the kind of digital camera.

Digital cameras typically capture images electronically and ultimately store the images as bits (ones and zeros) on a solid-state memory. Flash memory is the most common storage for digital cameras. Flash memory contains one or more electrically-erasable read-only-memory (EEPROM) integrated circuit chips that allow reading, writing, and block erasing.

Early digital cameras required the user to download or transfer the images from the flash memory within the digital camera to a personal computer (PC). A standard serial cable was most widely used. However, the limited transfer rate of the serial cable and the large size of the digital images made such serial downloads a patience-building experience. Serial downloads could easily take half an hour for only a few dozen images.

Digital camera manufacturers solved this problem by placing the flash memory chips on a small removable card. The flash-memory card could then be removed from the digital camera, much as film is removed from a standard camera. The flash-memory card could then be inserted into an appropriate slot in a PC, and the image files directly copied to the PC.

FIG. **1**A shows a flash memory card and adapter for transferring images from a digital camera to a PC. A user takes pictures with digital camera **14** that are stored in image files on flash memory chip(s). The flash memory chip is contained in CompactFlash card **16**, which can be removed from digital camera **14** by pressing a card-eject button. Thus CompactFlash card **16** contains the image files.

While some smaller hand-held computers or personal-digital-assistants (PDA) have slots that receive CompactFlash cards, most PCs do not. Laptop or notebook PCs have PC-card (earlier known as PCMCIA, Personal Computer Memory Card International Association) slots that can receive PCMCIA cards. Many functions have been placed on

PCMCIA cards, such as modems, Ethernet, flash memory, encryption keys, and even miniature hard drives.

CF-to-PCMCIA adapter **10** is a passive adapter that contains an opening that receives CompactFlash card **16**. FIG. **1**B shows CF-to-PCMCIA adapter **10** with CompactFlash card **16** inserted. Such CF-to-PCMCIA adapters **10** sell for as little as $5–10. CompactFlash is a trademark of SanDisk Corp. of Sunnyvale, Calif.

FIG. **1**C shows a PC connected to a PCMCIA reader. Most laptop and notebook PCs contain one or two PCMCIA slots **22** that CF-to-PCMCIA adapter **10** can fit into. Then the user merely has to copy the image files from CompactFlash card **16** (not shown) to the hard disk of PC **20**. Since high-speed parallel buses are used, transfer is rapid, about the same speed as accessing the hard disk. Thus a half-hour serial-cable transfer can be reduced to less than a minute with the $5 CF-to-PCMCIA adapter.

Desktop PCs usually do not have PCMCIA slots. Then PCMCIA reader **12** can be used. PCMCIA reader **12** accepts CF-to-PCMCIA adapter **10** and connects to PC **20** (not shown) through a parallel or high-speed Universal Serial Bus (USB) cable.

Multiple Flash-Card Formats

Although the CompactFlash card format is relatively small, being not much more than an inch square, other smaller cards have recently emerged. FIG. **2**A illustrates various formats of flash-memory cards used with digital cameras. Many digital cameras still use CompactFlash card **16**, which can be inserted into CF-to-PCMCIA adapter **10** for transfer to a PC. Other smaller, thinner formats have emerged and are used with some manufacturer's digital cameras. For example, SmartMedia card **24** is less than half an inch long, yet has enough flash memory capacity for dozens of images. SmartMedia-to-PCMCIA adapter **10'** is available commercially for about $60. The higher cost is believed to be due to a converter chip within adapter **10**. Also, different adapters **10** are required for different memory capacities of SmartMedia card **24**. SmartMedia is a trademark of the SSFDC Forum of Tokyo, Japan.

Other kinds of flash-memory cards that are being championed by different manufacturers include MultiMediaCard (MMC) **28** and the related Secure Digital Card (SD) **26**. MMC is controlled by MultiMediaCard Association that includes SanDisk Corp., Infineon Technologies, and others, while SD is controlled by the SD Group that includes Matsushita Electric Industrial Co., SanDisk Corporation, and Toshiba Corp., among others. Another emerging form factor from Sony Corporation is Memory Stick card **18**. Memory Stick has a PCMCIA/Floppy adapter while MMC has a floppy adapter.

The different physical shapes and pin arrangements of cards **24**, **26**, **28** and Memory Stick card **18** prevent their use in CF-to-PCMCIA adapter **10**. Indeed, most of these cards **24**, **26**, **28** have less than a dozen pins, while CompactFlash card **16** has a larger 50-pin interface. Furthermore, serial data interfaces are used in the smaller cards **24**, **26**, **28** while a parallel data bus is used with CompactFlash card **16**.

FIG. **2**B shows a Memory Stick-to-PCMCIA adapter using an active converter chip **11**. Memory Stick card **18** (not shown) fits into an opening in Memory Stick-to-PCMCIA adapter **15**, allowing adapter **15** and the Memory Stick to be plugged into a standard PCMCIA slot on a PC.

However, adapter **15** has an integrated circuit (IC) converter chip **11** within it. Converter chip **11** may be needed to convert the serial data format of Memory Stick card **18** to the parallel data format of a 68-pin PCMCIA slot. Inclusion of converter chip **11** in adapter **15** significantly increases the cost and complexity of adapter **15** compared to CF-to-PCMCIA adapter **10** which is a passive adapter without a converter chip.

While the advances in flash-memory card technology are useful, the many different card formats present a confusing array of interface requirements to a PC. Different adapters are needed for each of the card formats. PCMCIA card reader **12** can be replaced with other format readers, such as a SmartMedia Card reader, and even some multi-standard readers are available, such as a reader from Lexar Media that reads CompactFlash or SmartMedia in addition to PCMCIA.

The PCMCIA card interface (68-pins) has been around for a number of years and has been used extensively as an expansion slot for notebooks and other mobile computing devices. It is envisaged to use this popular interface to connect various devices such as SmartMedia, Memory Stick, MultimediaCard, Secure Digital card, Memory Stick V**2** (also called the Duo), USB expansion slot, etc., to a computing system, printer, PDA or other system, which has a mating 68 pin connector.

When such adapters (68-pin or any other pin/interface based adapter) are used to interchangeably connect to the computing system, a method of storing these adapters near the slot is desired (see FIG. **2**C).

FIG. **2**C illustrates a conventional bay **100** for storing the adapters (front view). The bay **100** includes an interface port **102** and slots **103**, **104** and **106** for storing adapters. The interface port **102** is the port to which dissimilar interfaces are connected via adapters. For example, a CompactFlash (or PCMCIA) interface can connect to a computing system, acting as the interface port for which other interfaces, such as SmartMedia, Memory Stick, Duo, USB, 1394, etc., can use adapters. The storage bay keeps all the adapters together.

In this type of bay, the upper slots are mounted right side up but the bottom slots require user to invert the media before inserting it into the slot. Since the slots are mounted on either side of a PCB (printed circuit board) the bottom slots are also very difficult to access. A new adapter for the upcoming smaller footprint Memory Stick (also called the Duo) is desired so as to mate it with 68-pin PCMCIA interface or 50-pin CompactFlash interface or any other similar interface. Therefore it is desirable to have a scheme wherein:

1. All slots are designed such that the flash media can be inserted face up into each slot.

2. There is comfortable separation space between the upper and lower row of slots.

What is desired is a universal adapter for flash-memory cards of several different formats. An adapter that accepts SmartMedia, MultiMediaCard, Secure Digital, and Memory Stick cards is desired. A flash-card reader with a single slot that accepts any format card using the adapter is desired. Special detection logic on the flash reader is desired to distinguish between the many flash-card formats. A low-cost passive adapter is desired that does not need an expensive converter chip. A multi-format reader is desired for a PC. A stand-alone flash reader is desired that can copy image files from flash cards without a PC.

What is further desired is an active adapter that can be used for interchangeably connecting different memory/memories to a device. For example, such a device could be a printer, a PDA device, or other device, which includes a slot for accepting a connector for a CompactFlash disk. It is known, for example, that many printers have a connector for a CompactFlash. Accordingly, what is needed is an active adapter, which addresses the above-identified problems.

It is also known that flash media is utilized in a variety of environments. Heretofore, the flash media is provided as a separate media to a device. In so doing, an array of different types of modules must be provided to allow for a connection to a device such as a digital camera, MP3 player or flash reader. It is desirable to provide a memory module that could be utilized with a variety of devices. The memory module must be compatible with existing standards and be capable of operating as a module.

Accordingly, what is also needed is a system and method for providing a plurality of memories to such a device without requiring multiple connectors or a controller within the memory module. The system should be cost effective, a simple modification and easily implementable into an existing device. What is further clearly needed is a controller that can work with multiple types of flash memory cards that have controllers, and also with flash memory cards that do not have controllers.

Furthermore, a controller IC, a system, and a method are needed to work with multiple types of flash memory cards that have controllers, and also with flash memory cards that do not have controllers.

SUMMARY OF THE INVENTION

A controller chip for coupling a computer system with a flash storage system is disclosed. The controller chip comprises an interface mechanism for determining whether the Flash storage system includes a controller and an adapter for providing the appropriate interface to the computer system to allow the computer system to communicate with the Flash storage system.

In a preferred embodiment, the flash storage system comprising at least a portion of a medium ID section; and a flash section, wherein the medium ID section contains specifications of the medium ID. Through the use of this system a plurality of different adapters and a flash storage system can be managed while utilizing the same hardware components.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1**A shows a flash memory card and adapter for transferring images from a digital camera to a PC.

FIG. **1**B shows a CF-to-PCMCIA adapter with CompactFlash card inserted.

FIG. **1**C shows a PC connected to a PCMCIA reader.

FIG. **2**A illustrates various formats of flash-memory cards used with digital cameras.

FIG. **2**B shows a Memory Stick-to-PCMCIA adapter using an active converter chip **11**.

FIG. **2**C illustrates a conventional bay for storing the adapters (front view).

FIG. **3**A shows a universal CompactFlash adapter that accepts SmartMedia, MultiMediaCard, Secure Digital, and Memory Stick flash-memory cards.

FIG. **3**B shows a CompactFlash reader that reads SmartMedia, MultiMediaCard, Secure Digital, and Memory Stick flash-memory cards through passive adapters to the CompactFlash form factor.

FIGS. **4**A–**4**E detail detection of the type of flash-memory card by the CompactFlash reader.

FIG. **4**A is an illustration of the CompactFlash reader interface in which the CE**2** and CE**2** pins are highlighted.

FIG. **4**B illustrates a CompactFlash card inserted into the connector for card-type detection.

FIG. **4**C illustrates a MultiMediaCard or Secure Digital card inserted into the connector for card-type detection.

FIG. **4**D illustrates a Memory Stick card inserted into the connector for card-type detection.

FIG. **4**E illustrates a SmartMedia card inserted into the connector for card-type detection.

FIG. **5** is a table of pin mappings for the SmartMedia, MMC/SD, and Memory Stick to CompactFlash adapters.

FIG. **6** is a diagram of a multi-slot embodiment of the flash-card reader.

FIG. **7** shows a flash-memory reader within a PC.

FIG. **8** shows a PC chassis with a flash-card reader in one of the drive bays.

FIG. **9** is a diagram of a stand-alone flash reader that accepts several formats of flash-memory cards and can copy images to a removable disk without being connected to a host PC.

FIG. **10** is a diagram of the converter chip for the flash-memory reader.

FIG. **11** shows a CompactFlash reader that reads SmartMedia, MultiMediaCard, Secure Digital, and Memory Stick flash-memory cards through passive IDE adapters to the CompactFlash form factor.

FIGS. **12**A–**12**E detail detection of the type of flash-memory card by the CompactFlash reader.

FIG. **12**A illustrates the CompactFlash reader interface with the CE**1** and CE**2** pins highlighted.

FIG. **12**B illustrates a CompactFlash card inserted into the connector for card-type detection.

FIG. **12**C illustrates a MultiMediaCard or Secure Digital card inserted into the connector for card-type detection.

FIG. **12**D illustrates a Memory Stick card inserted into the connector for card-type detection.

FIG. **12**E illustrates a SmartMedia card inserted into the connector for card-type detection.

FIG. **13** is a diagram of a multi-slot embodiment of the flash-card reader, which utilizes the IDE converter chip.

FIG. **14** shows a flash-memory reader within a PC, which utilizes the IDE converter chip.

FIG. **15** is a diagram of a stand-alone Flash reader with an IDE converter chip that accepts several formats of flash-memory cards and can copy images to a removable disk without being connected to a host PC.

FIG. **16** is a diagram of the IDE converter chip for the flash-memory reader.

FIG. **17** shows a CompactFlash reader system that reads SmartMedia, MultiMediaCard, Secure Digital, and Memory Stick flash-memory cards on the input side and interfaces to CompactFlash, IDE and PCMCIA on an output side.

FIG. **18** is a table showing the translator in between the flash media and the plurality of interfaces.

FIG. **19** is a block diagram of an active adapter chip in accordance with the present invention.

FIG. **20** is a table of pin mappings for the SmartMedia, MMC/SD, and Memory Stick to CompactFlash adapters.

FIG. **21** illustrates a SmartStack module.

FIG. **22** illustrates examples of the kinds of applications that can utilize the SmartStack module, such as a flash reader, digital camera or MP3 player.

FIG. **23** is a table that illustrates how a particular card will be detected by a device.

FIG. **24** is a table that illustrates addressing of the SmartStack module.

FIG. **24**A illustrates the relationship between SmartStack module address lines (S**0** . . . S**3**) and their equivalent pins in a CompactFlash card.

FIG. **25** illustrates a SmartStack module which includes the write protect mechanism, security area and biometric area.

FIG. **26** is a table that illustrates the setting of a secure area of data for the SmartStack module.

FIG. **27** illustrates adding a RAM to SmartStack module to improve performance.

FIG. **28** illustrates daisy-chaining a plurality of SmartStack modules in accordance with the present invention.

FIG. **29** illustrates a SmartStack module, which is an expansion bay.

FIG. **30** illustrates a system that is adaptable to a single media type.

FIG. **31** shows a cost-improved flash medium.

FIG. **32** shows various implementations of ID **4030**.

DETAILED DESCRIPTION

The present invention relates to an improvement in flash-memory card readers, and more particularly for interfacing several different types of flash memory cards to a device that includes a processor. It also relates generally to memory modules and more particularly to a memory module, which is coupled via a single connector. The following description is presented to enable one of ordinary skill in the art to make and use the invention as provided in the context of a particular application and its requirements. Various modifications to the preferred embodiment will be apparent to those with skill in the art, and the general principles defined herein may be applied to other embodiments. Therefore, the present invention is not intended to be limited to the particular embodiments shown and described, but is to be accorded the widest scope consistent with the principles and novel features herein disclosed.

Description of a Flash Reader for Reading Several Types of Flash-Memory Cards with or without a PC

The inventors have realized that a universal adapter can be constructed using the CompactFlash card form factor. A reader that reads CompactFlash cards can then read any of the other flash-memory cards that plug into the CompactFlash adapter. The adapters are simple, inexpensive passive adapters without a conversion chip.

The inventors have found a pin mapping from the smaller flash-card formats to CompactFlash that allows for easy detection of the type of flash-memory card inserted into the adapter. Detection of the type of flash-memory card is thus performed automatically by electronic detection by the CompactFlash reader. The CompactFlash reader is modified to perform this card-type detection. Signal conversion such as serial-to-parallel is performed by the CompactFlash reader rather than by the adapter. Adapter costs are reduced while CompactFlash reader cost is increased only slightly. The CompactFlash reader can use a single CompactFlash slot to read multiple flash-card types, including SmartMedia, MultiMediaCard, Secure Digital, Memory Stick, and CompactFlash.

In another embodiment, the CompactFlash reader is somewhat larger, and has multiple slots. The adapter is not needed in this embodiment. Instead, a slot is provided for each of the flash-memory card formats—SmartMedia, MultiMediaCard, Secure Digital, Memory Stick, and CompactFlash. A PCMCIA slot can also be added. This Compact-

Flash reader can be connected to the PC by a USB cable, or it can be located within the PC chassis.

In a third embodiment, the CompactFlash reader is a stand-alone device that can operate without a PC. A removable disk media such as a R/W CD-ROM is included. The CompactFlash reader copies images from the flash-memory card to the removable disk media. A simple interface is used; such as having the user presses a button to initiate image transfer.

Universal, Passive Adapters—FIGS. **3**A–B

FIG. **3**A shows a universal CompactFlash adapter that accepts SmartMedia, MultiMediaCard, Secure Digital, and Memory Stick flash-memory cards. Digital camera **14** stores images on flash memory that is in one of several card types. CompactFlash card **16** uses a 50-pin connector and transfers image data in a 16-bit parallel format.

SmartMedia card **24** is a smaller flash-memory card with a 22-pin interface and transfers data in an 8-bit parallel format. SmartMedia adapter **30** converts the 22-pin SmartMedia interface to fit within the 50-pin CompactFlash interface. When SmartMedia card **24** is plugged into SmartMedia adapter **30**, both can be plugged into a CompactFlash slot on a CompactFlash reader. Of course, ordinary CompactFlash readers will not be able to read SmartMedia card **24** since the CompactFlash reader requires special signal conversion.

MultiMediaCard **28** and Secure Digital card **26** are flash-memory cards with similar 9-pin interfaces. Serial data transfer is used through a single Data I/O pin. MMC/SD adapter **32** has an opening with a 9-pin connector to receive either MultiMediaCard **28** or Secure Digital card **26**. Once MultiMediaCard **28** or Secure Digital card **26** is inserted into MMC/SD adapter **32**, then MMC/SD adapter **32** can be inserted into a CompactFlash slot on a special CompactFlash reader. The CompactFlash reader then detects the card type and performs serial-to-parallel conversion.

Memory Stick card **18** is also a flash-memory card with 10-pin, serial-data interfaces, but is narrower and longer than MultiMediaCard **28** or Secure Digital card **26**. Memory Stick adapter **34** has an opening with a 10-pin connector to receive Memory Stick card **18**. Once Memory Stick card **18** is inserted, Memory Stick adapter **34** can itself be inserted into a CompactFlash slot on a special CompactFlash reader. The CompactFlash reader then detects the card type and performs serial-to-parallel conversion.

FIG. **3**B shows a CompactFlash reader **42** that reads SmartMedia, MultiMediaCard, Secure Digital, and Memory Stick flash-memory cards through passive adapters to the CompactFlash form factor. CompactFlash reader **42** has an opening or slot with 50-pin connector **44** that accepts CompactFlash card **16**. Converter chip **40** performs handshaking with CompactFlash card **16** and performs data transfer. CompactFlash reader **42** also connects to a PC over USB connector **46**. Converter chip **40** also controls the USB interface to the host PC, allowing image files to be transferred to the PC from CompactFlash card **16**.

CompactFlash reader **42** can also read other kinds of flash-memory cards. For example, MemoryStick adapter **34** allows Memory Stick card **18** to be read. Memory Stick adapter **34** has an opening that Memory Stick card **18** fits into, while Memory Stick adapter **34** itself fits into 50-pin connector **44**, since MemoryStick adapter **34** has the same form factor as a CompactFlash card.

SmartMedia card **24** can also be read by CompactFlash reader **42**, using SmartMedia adapter **30**. Likewise, MultiMediaCard **28** or Secure Digital card **26** can be read using MMC/SD adapter **32**.

Adapters **30**, **32**, **34** are passive adapters that only connect pins from the smaller flash-memory cards to the 50-pin CompactFlash connector. An active converter chip is not required, greatly reducing cost and complexity.

Detection of Card Type—FIGS. **4**A–E.

FIGS. **4**A–E detail detection of the type of flash-memory card by the CompactFlash reader. Since the same CompactFlash slot is used for many kinds of flash-memory cards, a detection method is useful so that the user doesn't have to explicitly indicate what type of flash-memory card is inserted into the CompactFlash reader.

The inventors have carefully examined the pins of the interfaces to the various flash-memory cards and have discovered that type-detection can be performed by examining two pins. Pins CE**1** and CE**2** are the chip enable pins of the 50-pin CompactFlash interface. These pins are normally inputs to the CompactFlash card and thus are driven by the CompactFlash reader. When the reader does not drive CE**1**, CE**2** to the inserted CompactFlash card, the CE**1**, CE**2** pins float or are pulled high by pull-up resistors.

Address pins are not present on the other kinds of flash-memory cards. Instead, the address and data are multiplexed. For MMC/SD and Memory Stick cards, the address is sent serially. Using the adapters, pins from the other flash-memory cards can be connected to the CompactFlash pins. Pins CE**1** and CE**2** are used to detect the type of card. For SmartMedia cards, the addresses are sent by using a special control sequence followed by 3or 4 bytes of starting address.

In FIG. **4**A, the CE**2**, CE**1** pins of the CompactFlash reader interface are highlighted. Converter chip **40** in the CompactFlash reader normally drives all **11** address pins in the CompactFlash interface when reading a CompactFlash card plugged into connector **44**. The CE**1** pin from the CompactFlash card plugs into connector cup **56**, while the CE**2** pin from the CompactFlash card plugs into connector cup **58** of 50-pin connector **44**.

Card-type detector **50** has two pull-up resistors added to lines CE**1**, CE**2**. Resistor **52** pulls line CE**1** high to power (Vcc) when neither converter chip **40** nor a card plugged into connector **44** drives line CE**1**. Likewise, resistor **54** pulls line CE**2** high when line CE**2** is not being actively driven. During detection mode, converter chip **40** is programmed to not drive lines CE**1**, CE**2** and instead use then as inputs to the detector logic.

In FIG. **4**B, a CompactFlash card is inserted into the connector for card-type detection. CompactFlash card **16** is plugged into connector **44**. Since CE**1** and CE**2** are inputs to CompactFlash card **16**, they are not driven by CompactFlash card **16**. During detection mode, converter chip **40** also does not drive pins CE**1**, CE**2**. Thus lines CE**1**, CE**2** are left floating and are each pulled high by resistors **52**, **54**.

Detection logic in converter chip **40** reads card-select pins CD**0**, CD**1** to detect the presence of a flash-memory card. When a new card is present, detection logic then reads pins CE**1**, CE**2** as inputs. Both inputs are high. The detection logic in converter chip **40** recognizes the HH state of CE**1**, CE**2** as indicating that a CompactFlash card is plugged into connector **44**. Converter chip **40** then exits detection mode and configures its interface to connector **44** for the 50-pin CompactFlash interface as shown later in FIG. **5**.

In FIG. **4**C, a MultiMediaCard or Secure Digital card is inserted into the connector for card-type detection. MMC/

SD card **28** (not shown) is plugged into MMC/SD adapter **32**, which is plugged into connector **44**.

Converter chip **40** does not drive pins CE**1**, CE**1** during detection mode. Thus pin CE**2** floats and is pulled high by resistor **54**.

The CE**1** pin is driven low by the MMC card.

Detection logic in converter chip **40** reads card-select pins CD**0**, CD**1** to detect the presence of a flash-memory card. When a new card is present, detection logic then reads pins CE**1**, CE**2** as inputs. While CE**1** is low, CE**2** is high. The detection logic in converter chip **40** recognizes the LH state of CE**1**, CE**2** as indicating that a MMC or SD card is plugged into connector **44**. Converter chip **40** then exits detection mode and configures its interface to connector **44** for the 9-pin MMC/SD interface as shown later in FIG. **5**.

In FIG. **4**D, a Memory Stick card is inserted into the connector for card-type detection. Memory Stick card **18** (not shown) is plugged into Memory Stick adapter **30** which is plugged into connector **44**. The adapter **30** does not connect pins CE**1**, CE**2** from the CompactFlash interface to any pins on the Memory Stick card. Adapter **30** internally connects pin CE**2** from the CompactFlash interface to the ground pin on the CompactFlash interface.

The Memory Stick card does not drive either pin CE**2**, CE**1**, although adapter **34** drives pin CE**2** low. Likewise, converter chip **40** does not drive pins CE**2**, CE**1** during detection mode. Pin CE**1** floats and is pulled high by resistor **52**.

Detection logic in converter chip **40** reads card-select pins CD**0**, CD**1** to detect the presence of a flash-memory card. When a new card is present, detection logic then reads pins CE**1**, CE**2** as inputs. While CE**1** is high, CE**2** is low. The detection logic in converter chip **40** recognizes the HL state of CE**1**, CE**2** as indicating that a Memory Stick card is plugged into connector **44**. Converter chip **40** then exits detection mode and configures its interface to connector **44** for the Memory Stick interface as shown later in FIG. **5**.

In FIG. **4**E, a SmartMedia card is inserted into the connector for card-type detection. SmartMedia card **24** (not shown) is plugged into SmartMedia adapter **34**, which is plugged into connector **44**.

Detection logic in converter chip **40** reads card-select pins CD**0**, CD**1** to detect the presence of a flash-memory card. When a new card is present, detection logic then reads pins CE**1**, CE**2** as inputs. Both pins CE**1**, CE**2** are low. The detection logic in converter chip **40** recognizes the LL state of CE**1**, CE**2** as indicating that a SmartMedia card is plugged into connector **44**.

Pin Mapping—FIG. **5**

FIG. **5** is a table of pin mappings for the SmartMedia, MMC/SD, and Memory Stick to CompactFlash adapters. The pin numbers for the smaller interfaces for SmartMedia, MMC/SD, and Memory Stick are not shown but can be in any order or designation. The adapter connects the proper pin on the smaller interface to the CompactFlash pin number shown in FIG. **5**. Simple wiring such as individual wires, flat cables, printed-circuit board (PCB), or wiring traces can be used.

The ground pins on the smaller interfaces are connected to CompactFlash pins **1** and **50**. Power pins are connected to CompactFlash pins **13**, **38**. Pins **25**, **26** are the card-detect signals for CompactFlash, which the adapters connect to the card-detect signals on all smaller interfaces.

The CompactFlash connectors use pins **2**–**6**, **21**–**23**, **27**–**31**, and **47**–**49** for the 16-bit parallel data bus to the CompactFlash card. Pins **8**, **10**–**12**, and **14**–**20** form a separate 11-bit address bus. The separate data and address buses provide for rapid random addressing of CompactFlash cards. Other control signals include pins **6**, **32** chip enables, pin **9** output enable, pin **36** write enable, interrupt pin **37**, reset pin **41**, and register REG pin **44**. REG pin **44** is the Attribute Memory Select, defined based on the CF mode of operation, i.e. PCMCIA I/O mode, IDE or PCMCIA Memory Mode. Several pins in the 50-pin interface are not connected.

The smaller SmartMedia interface also has a parallel data bus of 8 bits. These are mapped to pins **2**–**6**, and **21**–**23** of the CompactFlash interface to match the CompactFlash D0:7 signals. While no separate address bus is provided, address and data are multiplexed. Control signals for latch enables, write enable and protect, output enable, and ready handshake are among the control signals. Output enable—OE and write enable—WE are mapped to the same function pins **9**, **36** of the CompactFlash interface. The total number of pins in the SmartMedia interface is 22.

The Memory Stick and MMC/SD flash-memory-card interfaces are smaller still, since parallel data or address busses are not present. Instead, serial data transfers occur through serial data pin DIO, which is mapped to pin **19** (CE**2**). Data is clocked in synchronization to clock SCLK on pin **18**. A command signal CMD or BS occupies pin **20** (CE**1**). The MMC/SD and Memory Stick interfaces require only 6 pins plus power and ground.

Detection logic in converter chip **40** reads card-select pins CD**0**, CD**1** to detect the presence of a flash-memory card. When a new card is present, detection logic then reads pins CE**1**, CE**2** as inputs to determine the card type. The pull-up resistors of FIG. **4**A together with wiring inside the adapter and the card's behavior determines whether CE**1**, CE**2** are pulled low by the adapter or pulled high by the pull-up resistors.

Multi-Slot Multi-Flash-Card Reader—FIG. **6**

FIG. **6** is a diagram of a multi-slot embodiment of the flash-card reader. While the single-slot embodiment of FIG. **3**B results in the smallest physical design, somewhat larger flash-card readers can be made that have separate slots for each type of flash-memory card, rather than a single slot. This negates the need for the adapters or with some slots with multiple connectors.

Four connectors are provided in flash reader **42**: a 50-pin CompactFlash connector **62** that fits CompactFlash card **16**, a 9 pin MMC/SD connector **64** that fits MultiMediaCard **28** or a Secure Digital card **26**, a 22-pin SmartMedia connector **66** that fits SmartMedia card **24**, and a 10-pin Memory Stick connector **68** that fits Memory Stick card **18**. Each of the four connectors **62**, **64**, **66**, **68** route their signals to converter chip **40**. Converter chip **40** detects when a flash-memory card has been inserted into one of the connectors **62**, **64**, **66**, **68** and configures itself to read files from the inserted card using the pin interface of FIG. **5** corresponding to the card type.

Converter chip **40** executes various routines to perform handshaking with the flash-memory cards and accept data, either serially or in parallel. The data is buffered and then sent to the host PC **20** through USB connector **46**. Converter chip **40** generates the appropriate USB-interface signals to transfer the data to host PC or any computing system **20**.

Having separate connectors **62**, **64**, **66**, **68** with separate slots in flash reader **42** allows for card-to-card transfers. For example, images or other files from Memory Stick card **18** could be transferred to CompactFlash card **16** by converter chip **40** reading serial data from Memory Stick card inserted

into connector **68**, converting to parallel, and writing to connector **62** and CompactFlash card **16**. Each of the flash-memory cards in connectors **62**, **64**, **66**, **68** can be assigned a different drive letter by the operating system, such as E:, F:, G:, and H:.

In this embodiment, flash reader **42** is contained in an external housing that connects to host PC **20** through a USB cable. Of course, other cables and interfaces such as IEEE 1394 FireWire may be substituted.

Flash Reader Within PC—FIGS. **7–8**

FIG. **7** shows a flash-memory reader within a PC. Four slots and four connectors are provided in flash reader **42**. A 50-pin CompactFlash connector **62** fits CompactFlash card **16**, a 9-pin MMC/SD connector **64** fits MultiMediaCard **28** or a Secure Digital card **26**, a 22-pin SmartMedia connector **66** fits SmartMedia card **24**, and a 10-pin Memory Stick connector **68** fits Memory Stick card **18**.

Each of the four connectors **62**, **64**, **66**, **68** route their signals to converter chip **40**. Converter chip **40** detects when a flash-memory card has been inserted into one of the connectors **62**, **64**, **66**, **68** and configures itself to read files from the inserted card using the pin interface of FIG. **5** corresponding to the card type. Each of the flash-memory cards in connectors **62**, **64**, **66**, **68** can be assigned a different drive letter by the operating system, such as E:, F:, G:, and H:.

Converter chip **40** executes various routines to perform handshaking with the flash-memory cards and accept data, either serially or in parallel. The data is buffered and then sent to the CPU **21** in PC **20** through an internal USB bus. Converter chip **40** generates the appropriate USB-interface signals to transfer the data to CPU **21**.

FIG. **8** shows a PC chassis with a flash-card reader **42** in one of the drive bays. PC **20** is enclosed by a chassis or case that has several drive bays allowing the user or manufacturer to insert peripherals such as hard and floppy disk drives, CD-ROM and DVD drives, and tape drives. HDD bay **72** contains a hard-disk drive, while FDD bay **74** contains a floppy disk drive. These are connected by cables to cards inserted into a USB, ATA, or other expansion bus connectors on the motherboard.

Flash reader **42** is inserted into one of the drive bays. The four slots face forward, allowing the user to insert flash-memory cards into flash reader **42** much as a floppy disk is inserted into the floppy-disk drive in FDD bay **74**.

Flash reader **42** can be installed by the user from a kit purchased at a store, or it can be pre-installed by an original-equipment manufacturer (OEM) or retailer. The user can easily transfer digital images from a digital camera, regardless of the type of flash-card used by the camera, due to the many different formats of flash-memory cards read by flash reader **42**. While Digital cameras are used as an illustration, the concept applies to movement of data.

Flash Reader—FIG. **9**

FIG. **9** is a diagram of a stand-alone flash reader **80** that accepts several formats of flash-memory cards and can copy images to a removable disk without being connected to a host PC. Digital photographers may not always have their PCs nearby. While extra flash-memory cards can be purchased and swapped in the digital camera, these flash-memory cards are somewhat expensive, especially when many high-resolution images are captured. Especially during a long trip away from the PC, the user may be limited by the capacity of the flash-memory cards.

Flash reader **80** has four slots and four connectors are provided in Flash reader **80**. A 50-pin CompactFlash connector **62** fits CompactFlash card **16**, a 9-pin MMC/SD connector **64** fits MultiMediaCard **28** or a Secure Digital card, a 22-pin SmartMedia connector **66** fits SmartMedia card **24**, and a 10-pin Memory Stick connector **68** fits Memory Stick card **18**.

Each of the four connectors **62**, **64**, **66**, **68** route their signals to converter chip **40**. Converter chip **40** detects when a flash-memory card has been inserted into one of the connectors **62**, **64**, **66**, **68** by sensing card select lines CD**0**, CD**1** and configures itself to read files from the inserted card using the pin interface of FIG. **5** corresponding to the card type.

Converter chip **40** executes various routines to perform handshaking with the flash-memory cards and accept data, either serially or in parallel. The data is buffered and then sent either to host PC **20** through USB connector **46** or to removable mass storage **70**. Converter chip **40** generates the appropriate USB-interface signals to transfer the data to host PC **20**. Converter chip **40** also generates the control signals for removable mass storage **70**, allowing the image data read from the flash-memory card to be written to removable disk **76**. Removable disk **76** could be a standard or a high-density floppy diskette, a tape drive, a write-able CD-R/W disk, or other proprietary media such as LS120 by Imation of Oakdale, Minn., or ZIP drives by Iomega Corp. of Roy, Utah.

Each of the flash-memory cards in connectors **62**, **64**, **66**, **68** can be assigned a different drive letter by the operating system, such as E:, F:, G:, and H:. Removable mass storage **70** can also be signed a drive letter.

When Flash reader **80** is not attached to host PC **20**, image files may still be copied to removable mass storage **70**. Flash reader **80** may be carried along on a trip by the user, allowing the user to download image files to removable disk **76**. Since removable disk **76** ordinarily has a much higher capacity than the flash-memory cards, many pictures may be captured when no access to host PC **20** is available. Flash reader **80** can be provided with battery power or with its own AC converter.

Flash reader **80** is provided with a simple user interface, including light-emitting diode LED **78** and button **79**. When the user inserts a flash-memory card into one of connectors **62**, **64**, **66**, **68**, and removable disk **76** is inserted into removable mass storage **70**, the user presses button **79**. This activates converter chip **40**, which determines which of connectors **62**, **64**, **66**, **68** have a memory card inserted, and copies the image files to removable mass storage **70**. LED **78** can be programmed to blink during the copying process, and remain lit when the copying is complete, or vice-versa. This provides a simple visual indication to the user of the copying progress. Errors can be indicated with additional LED indicator lamps, or other blinking arrangements or colors.

Converter Chip—FIG. **10**

FIG. **10** is a diagram of the converter chip **40** for the flash-memory reader. Converter chip **40** can be implemented as a commercially available micro-controller chip that is programmed to read and write I/O pins that are connected to the flash-memory-card connectors and USB interface. Several different control and transfer routines are written and programmed into RAM/ROM **94**. CPU **92** then executes these routines. A high-level scanning routine can sense when a flash-memory card is inserted. CPU **92** can then begin execution of another routine specific to that type of flash-memory card. Transfer and handshake sub-routines can then be called.

General-purpose input-output GPIO **99** provides registers or I/O ports that drive external I/O pins of converter chip **40**, or read the logic-levels or voltages on input pins to converter chip **40**. CPU **92** can read registers in GPIO **99** that are written by control signals that are coupled to I/O pins of converter chip **40** from connectors **62**, **64**, **66**, **68** (not shown). Control signals to the flash-memory cards can be switched high or low by writing a 1 or a 0 to a register for that control signal in GPIO **99**.

Timers **96** are useful for asserting control signals for a required amount of time. For example, a control signal may need to be asserted for a specified number of microseconds. CPU **92** can write a 1 to a register in GPIO **99** and start a timer in timers **96**. Timer **6** can send an interrupt to CPU **96** when the specified time has elapsed, or CPU **92** can continuously or periodically poll timers **96** to determine when the specified time has elapsed. Then CPU **92** can write a 0 to the register in GPIO **99**, causing the control signal to transition from 1 to 0.

Shifter **98** is connected to the data and clock signals from connectors **64**, **68**. When data is read from the flash-memory card, a clock is pulsed to synchronize the data transfer. Shifter **98** clocks in one bit (serial) or word (parallel) of data for each clock pulse.

A cyclical-redundancy-check (CRC) can be performed on the data to detect errors. CPU **92** can request re-transmission of data from the flash-memory card when an error is detected.

Data read by shifter **98** can be sent over internal bus **90** to be stored in a buffer in RAM/ROM **94**. Later, CPU **92** can execute a routine to transfer this data from RAM/ROM **94** to USB interface **100**. USB interface **100** then transmits the data over an external USB link to a host PC. When a removable mass storage is present, some of the I/O pins from GPIO **99** can connect to the removable mass storage, or a separate disk controller can be included on converter chip **40**.

Advantages of a Flash Reader for Reading Several Types of Flash-Memory Cards with or without a PC

A universal adapter for flash-memory cards accepts cards of several different formats. The adapter accepts SmartMedia, MultiMediaCard, Secure Digital, and Memory Stick cards. The flash-card reader with a single slot accepts any format card using the adapter. Special detection logic on the flash reader distinguishes between the many flash-card formats. The low-cost passive adapter does not need an expensive converter chip. A multi-format reader is ideal for use with a PC. However, a stand-alone flash reader can copy image files from flash cards without a PC. Additionally, preparation of media for use in devices (format and erase operations) can be done using this reader.

A universal adapter is constructed using the CompactFlash card form factor. A reader that reads CompactFlash cards can then read any of the other flash-memory cards that plug into the CompactFlash adapter. The adapters are simple, inexpensive passive adapters without a conversion chip.

The disclosed pin mapping from the smaller flash-card formats to CompactFlash allows for easy detection of the type of flash-memory card inserted into the adapter. Detection of the type of flash-memory card is thus performed automatically by electronic detection by the CompactFlash reader. The CompactFlash reader is modified to perform this card-type detection. Signal conversion such as serial-to-parallel is performed by the CompactFlash reader rather than by the adapter. Adapter costs are reduced while CompactFlash reader cost is increased only slightly. The CompactFlash reader can use a single CompactFlash slot to read multiple flash-card types, including SmartMedia, MultiMediaCard, Secure Digital, Memory Stick, and CompactFlash.

Alternate Embodiments of a Flash Reader for Reading Several Types of Flash-Memory Cards with or without a PC

Several other embodiments are contemplated by the inventors. Different flash-card formats can be supported such as Smart Cards, and more or less than the four slots shown in the multi-card flash reader can be included. Other adapters can be used for newer flash formats for the single-slot CompactFlash reader. Any device that needs Control Bus, Clock, Data Bus and Address Bus can be designed to fit into this slot. Examples of such devices include (but are not limited to) DSL Modems, Fingerprint security devices, Miniature Hard disks, etc.

While the invention has been described as connecting to a personal computer PC host, the host may also be an Apple computer such as the iMAC or G3. The host may also be a SUN computer, or any host computer using USB or IDE interfaces. The invention can also apply to Personal Digital Assistants (PDAs) such as by Palm Computer or other handheld appliances, such as a Cell phone with USB capability.

The term "CompactFlash reader" has been used for simplicity, since digital images are often read from the flash-memory card and then written to the PC. However, the CompactFlash reader is capable of reading files from the PC or from another flash-memory card and writing the file to the flash-memory card. Thus the CompactFlash reader is really a reader/writer.

In another embodiment, the CompactFlash reader is somewhat larger, and has multiple slots. The adapter is not needed in this embodiment. Instead, a slot is provided for each of the flash-memory card formats—SmartMedia, MultiMediaCard, Secure Digital, Memory Stick, and CompactFlash. A PCMCIA slot can also be added. This CompactFlash reader can be connected to the PC by a USB cable, or it can be located within the PC chassis.

In a third embodiment, the CompactFlash reader is a stand-alone device that can operate without a PC. A removable disk media such as a R/W CD-ROM is included. The CompactFlash reader copies images from the flash-memory card to the removable disk media. A simple interface is used; such as having the user presses a button to initiate image transfer. Additionally a display of the file copy process can be done on a display device such as an LCD screen. The foregoing description of the embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed. Many modifications and variations are possible in light of the above teaching. It is intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto.

Description of Improved Flash Reader for Reading Several Types of Flash-Memory Cards with or without a PC

A universal adapter was disclosed that can be constructed using the CompactFlash card form factor. A reader that reads CompactFlash cards can then read any of the other flash-memory cards that plug into the CompactFlash adapter. The adapters are simple, inexpensive passive adapters without a conversion chip.

Although the above-identified compact flash reader operates effectively for its stated purpose, it cannot be utilized with an Integrated Devices Electronics (IDE) interface

effectively in certain circumstances. It is desirable that a compact flash reader be utilized with an IDE interface for several reasons. Firstly, the IDE interface is a proven interface and an easy interface to design to, for devices such as digital cameras, printers, etc., which may want to embed this chip in their devices. Secondly, the IDE interface is extremely fast and will boost the transfer rates of the devices. IDE ports are freely available on most systems (since only 2 or at the most 3 of the total of 4 IDE ports are used up). Finally, attaching to the front panel of an IDE interface is possible for 100% of all PCs/Macs, etc., whereas an internal expansion slot for USB is utilized in many newer systems.

A system and method in accordance with the present invention allows an IDE interface to replace the USB interface. This will allow a flash reader to be built that could be put into the front panel of a PC in a manner that is similar to placing a CDROM into the front panel. To further describe the features of the present invention, refer now to the following description.

Universal, Passive Adapters

FIG. **11** shows a CompactFlash reader that reads SmartMedia, MultiMediaCard, Secure Digital, and Memory Stick flash-memory cards through passive IDE adapters to the CompactFlash form factor. CompactFlash reader **42** has an opening or slot with 50-pin connector **44** that accepts CompactFlash card **16**. An IDE converter chip **140** performs handshaking with CompactFlash card **16** and performs data transfer. CompactFlash reader **42** also connects to a PC over IDE connector **146**. The IDE converter chip **140** also controls the IDE interface to the host PC, allowing image files to be transferred to the PC from CompactFlash card **16**.

Other kinds of flash-memory cards can also be read by CompactFlash reader **42**. For example, MemoryStick adapter **34** allows Memory Stick card **18** to be read. Memory Stick adapter **34** has an opening that Memory Stick card **18** fits into, while Memory Stick adapter **34** itself fits into 50-pin connector **44**, since adapter **34** has the same form factor as a CompactFlash card.

SmartMedia card **24** can also be read by CompactFlash reader **42**, using SmartMedia adapter **30**. Likewise, MultiMediaCard **28** or Secure Digital card **26** can be read using MMC/SD adapter **32**.

Adapters **30**, **32**, **34** are passive adapters that only connect pins from the smaller flash-memory cards to the 50-pin CompactFlash connector. An active converter chip is not required, greatly reducing cost and complexity.

Detection of Card Type

FIGS. **12**A–E detail detection of the type of flash-memory card by the CompactFlash reader. Since the same CompactFlash slot is used for many kinds of flash-memory cards, a detection method is useful so that the user doesn't have to explicitly indicate what type of flash-memory card is inserted into the CompactFlash reader.

The inventors have carefully examined the pins of the interfaces to the various flash-memory cards and have discovered that type-detection can be performed by examining two pins. Pins CE**1** and CE**2** are the chip enable pins for addressing the 50-pin CompactFlash interface. These pins are normally inputs to the CompactFlash card and thus are driven by the CompactFlash reader. When the reader does not drive CE**1**, CE**2** to the inserted CompactFlash card, the CE**1**, CE**2** pins float or are pulled high by pull-up resistors.

Address pins are not present on the other kinds of flash-memory cards. Instead, the address and data are multiplexed. For MMC/SD and Memory Stick, the address is sent serially. Using the adapters, pins from the other flash-memory cards can be connected to the CompactFlash pins. Pins CE**1** and CE**2** are used to detect the type of card. For SmartMedia, the addresses are sent by using a special control sequence followed by 3 or 4 bytes of starting address.

In FIG. **12**A, the CE**1**, CE**2** pins of the CompactFlash reader interface are highlighted. The IDE converter chip **140** in the CompactFlash reader normally drives all **11** address pins in the CompactFlash interface when reading a CompactFlash card plugged into connector **44**. The CE**1** pin from the CompactFlash card plugs into connector cup **156**, while the CE**2** pin from the CompactFlash card plugs into connector cup **158** of 50-pin connector **44**.

Card-type detector **150** has two pull-up resistors added to lines CE**1**, CE**2**. Resistor **152** pulls line CE**1** high to power (Vcc) when neither the IDE converter chip **140** nor a card plugged into connector **44** drives line CE**1**. Likewise, resistor **154** pulls line CE**2** high when line CE**2** is not being actively driven. During detection mode, the IDE converter chip **140** is programmed to not drive lines CE**1**, CE**2** and instead use then as inputs to the detector logic.

In FIG. **12**B, a CompactFlash card is inserted into the connector for card-type detection. CompactFlash card **16** is plugged into connector **44**. Since CE**1** and CE**2** are inputs to CompactFlash card **16**, they are not driven by CompactFlash card **16**. During detection mode, the IDE converter chip **140** also does not drive pins CE**1**, CE**2**. Thus lines CE**1**, CE**2** are left floating and are each pulled high by resistors **152**, **154**.

Detection logic in the IDE converter chip **140** reads card-select pins CD**0**, CD**1** to detect the presence of a flash-memory card. When a new card is present, detection logic then reads pins CE**1**, CE**2** as inputs. Both inputs are high. The detection logic in the IDE converter chip **140** recognizes the HH state of CE**1**, CE**2** as indicating that a CompactFlash card is plugged into connector **44**. The IDE converter chip **140** then exits detection mode and configures its interface to connector **44** for the 50-pin CompactFlash interface as shown in FIG. **5**.

In FIG. **12**C, a MultiMediaCard or Secure Digital card is inserted into the connector for card-type detection. MultiMediaCard **28** (not shown) and Secure Digital card **26** (not shown) are plugged into MMC/SD adapter **32** which is plugged into connector **44** (not shown).

The IDE converter chip **140** does not drive pins CE**2**, CE**1** during detection mode. Thus pin CE**2** floats and is pulled high by resistor **154**. The CE**1** pin is driven low by the MMC card.

Detection logic in the IDE converter chip **140** reads card-select pins CD**0**, CD**1** to detect the presence of a flash-memory card. When a new card is present, detection logic then reads pins CE**1**, CE**2** as inputs. While CE**1** is low, CE**2** is high. The detection logic in the IDE converter chip **140** recognizes the LH state of CE**1**, CE**2** as indicating that a MMC or SD card is plugged into connector **44**. The IDE converter chip **140** then exits detection mode and configures its interface to connector **44** for the 9-pin MMC/SD interface as shown in FIG. **5**.

In FIG. **12**D, a Memory Stick card is inserted into the connector for card-type detection. Memory Stick card **18** (not shown) is plugged into Memory Stick adapter **34** which is plugged into connector **44**. The adapter **34** does not connect pins CE**1**, CE**2** from the CompactFlash interface to any pins on the Memory Stick card. Adapter **34** internally connects pin CE**2** from the CompactFlash interface to the ground pin on the CompactFlash interface.

The Memory Stick card does not drive either pin CE2, CE1, although adapter **34** drives pin CE2 low. Likewise, the IDE converter chip **140** does not drive pins CE2, CE1 during detection mode. Pin CE1 floats and is pulled high by resistor **152**.

Detection logic in the IDE converter chip **140** reads card-select pins CD0, CD1 to detect the presence of a flash-memory card. When a new card is present, detection logic then reads pins CE1, CE2 as inputs. While CE1 is high, CE2 is low. The detection logic in the IDE converter chip **140** recognizes the HL state of CE1, CE2 as indicating that a Memory Stick card is plugged into connector **44**. The IDE converter chip **140** then exits detection mode and configures its interface to connector **44** for the Memory Stick interface as shown in FIG. **5**.

In FIG. **12**E, a SmartMedia card is inserted into the connector for card-type detection. SmartMedia card **24** (not shown) is plugged into SmartMedia adapter **30**, which is plugged into connector **44**.

Detection logic in the IDE converter chip **140** reads card-select pins CD0, CD1 to detect the presence of a flash-memory card. When a new card is present, detection logic then reads pins CE1, CE2 as inputs. Both pins CE1, CE2 are low. The detection logic in the IDE converter chip **140** recognizes the LL state of CE1, CE2 as indicating that a SmartMedia card is plugged into connector **44**. Again, this mapping shall be exemplary only, and many variations may be used instead, without departing from the spirit of the invention.

Pin Mapping

Referring back to FIG. **5**, a table of pin mappings for the SmartMedia, MMC/SD, and Memory Stick to CompactFlash adapters is shown. The pin numbers for the smaller interfaces for SmartMedia, MMC/SD, and Memory Stick are not shown but can be in any order or designation. The adapter connects the proper pin on the smaller interface to the CompactFlash pin number shown in FIG. **5**. Simple wiring such as individual wires, flat cables, printed-circuit board (PCB), or wiring traces can be used.

The ground pins on the smaller interfaces are connected to CompactFlash pins **1** and **50**. Power pins are connected to CompactFlash pins **13**, **38**. Pins **25**, **26** are the card detect signals for CompactFlash, which the adapters connect to the card-detect signals on all smaller interfaces.

The CompactFlash connectors use pins **2–6**, **21–23**, **27–31**, and **47–49** for the 16-bit parallel data bus to the CompactFlash card. Pins **8**, **10–12**, and **10–20** form a separate 11-bit address bus. The separate data and address buses provide for rapid random addressing of CompactFlash cards. Other control signals include pins **6**, **32** chip enables, pin **9** output enable, pin **36** write enable, interrupt pin **37**, reset pin **41**, and register REG pin **44**. REG pin **44** is the Attribute Memory Select, defined based on the CF mode of operation, i.e. PCMCIA I/O mode, IDE or PCMCIA Memory Mode. Several pins in the 50-pin interface are not connected.

The smaller SmartMedia interface also has a parallel data bus of 8 bits. These are mapped to pins **2–6**, and **21–23** of the CompactFlash interface to match the CompactFlash D0:7 signals. While no separate address bus is provided, address and data are multiplexed. Control signals for latch enables, write enable and protect, output enable, and ready handshake are among the control signals. Output Enable (OE) and Write Enable (WE) are mapped to the same function pins **9**, pin **36** of the CompactFlash interface. The total number of pins in the SmartMedia interface is 22.

The Memory Stick and MMC/SD flash-memory-card interfaces are smaller still, since parallel data or address busses are not present. Instead, serial data transfers occur through serial data pin DATAIO, which is mapped to pin **19** (A1 Data is clocked in synchronization to clock SERCLK on pin **18**. A command signal CMD or BITSET occupies pin **20** (A0). The MMC/SD and Memory Stick interfaces require only 6 pins plus power and ground. Others are unused.

Detection logic in the IDE converter chip **140** reads card-select pins CD0, CD1 to detect the presence of a flash-memory card. When a new card is present, detection logic then reads pins CE1, CE2 as inputs to determine the card type. The pull-up resistors of FIG. **12**A together with wiring inside the adapter and the card's behavior determines whether CE1, CE2 are pulled low by the adapter or pulled high by the pull-up resistors.

Multi-Slot Multi-Flash-Card Reader

FIG. **13** is a diagram of a multi-slot embodiment of the flash-card reader, which utilizes the IDE converter chip. While the single-slot embodiment of FIG. **11** results in the smallest physical design, somewhat larger flash-card readers can be made that have separate slots for each type of flash-memory card, rather than a single slot. This negates the need for the adapters.

Four connectors are provided in flash reader **42**: a 50-pin CompactFlash connector **162** that fits CompactFlash card **16**, a 9 pin MMC/SD connector **164** that fits MultiMediaCard **28** or a Secure Digital card, a 22-pin SmartMedia connector **166** that fits SmartMedia card **24**, and a 10-pin Memory Stick connector **168** that fits Memory Stick card **18**.

Each of the four connectors **162**, **164**, **166**, **168** route their signals to the IDE converter chip **140**. The IDE converter chip **140** detects when a flash-memory card has been inserted into one of the connectors **162**, **164**, **166**, **168** and configures itself to read files from the inserted card using the pin interface of FIG. **5** corresponding to the card type.

The IDE converter chip **140** executes various routines to perform handshaking with the flash-memory cards and accept data, either serially or in parallel. The data is buffered and then sent to the host PC **20** through IDE connector **146**. The IDE converter chip **140** generates the appropriate IDE-interface signals to transfer the data to host PC **20**.

Having separate connectors **162**, **164**, **166**, **168** with separate slots in flash reader **42** allows for card-to-card transfers. For example, images or other files from Memory Stick card **18** could be transferred to CompactFlash card **16** by the IDE converter chip **140** reading serial data from Memory Stick inserted into connector **168**, converting to parallel, and writing to connector **162** and CompactFlash card **16**. Each of the flash-memory cards in connectors **162**, **164**, **166**, **168** can be assigned a different drive letter by the operating system, such as E:, F:, G:, and H:.

In this embodiment, flash reader **42** is contained in an external housing that connects to host PC **20** through an IDE cable. Of course, other cables and interfaces such as IEEE 1394 FireWire may be substituted.

Flash Reader within PC

FIG. **14** shows a flash-memory reader within a PC, which utilizes the IDE converter chip. Four slots and four connectors are provided in flash reader **42**. A 50-pin CompactFlash connector **162** fits CompactFlash card **16**, a 9-pin MMC/SD connector **164** fits MultiMediaCard **28** or a Secure Digital card, a 22-pin SmartMedia connector **166** fits SmartMedia card **24**, and a 10-pin Memory Stick connector **168** fits Memory Stick card **18**.

Each of the four connectors **162**, **164**, **166**, **168** route their signals to the IDE converter chip **140**. The IDE converter chip **140** detects when a flash-memory card has been inserted into one of the connectors **162**, **164**, **166**, **168** and configures itself to read files from the inserted card using the pin interface of FIG. **5** corresponding to the card type. Each of the flash-memory cards in connectors**12**, **164**, **166**, **168** can be assigned a different drive letter by the operating system, such as E:, F:, G:, and H:.

The IDE converter chip **140** executes various routines to perform handshaking with the flash-memory cards and accept data, either serially or in parallel. The data is buffered and then sent to the CPU **21** in PC **20** through an internal IDE-interface bus. The IDE converter chip **140** generates the appropriate IDE-interface signals to transfer the data to CPU **21**.

Flash Reader

FIG. **15** is a diagram of a stand-alone Flash reader with an IDE converter chip that accepts several formats of flash-memory cards and can copy images to a removable disk without being connected to a host PC. Digital photographers may not always have their PCs nearby. While extra flash-memory cards can be purchased and swapped in the digital camera, these flash-memory cards are somewhat expensive, especially when many high-resolution images are captured. Especially during a long trip away from the PC, the user may be limited by the capacity of the flash-memory cards.

Flash reader **180** has four slots and four connectors are provided in Flash reader **180**. A 50-pin CompactFlash connector **162** fits CompactFlash card **16**, a 9-pin MMC/SD connector **164** fits MultiMediaCard **28** or a Secure Digital card, a 22-pin SmartMedia connector **166** fits SmartMedia card **24**, and a 10-pin Memory Stick connector **168** fits Memory Stick card **18**.

Each of the four connectors **162**, **164**, **166**, **168** route their signals to the IDE converter chip **140**. The IDE converter chip **140** detects when a flash-memory card has been inserted into one of the connectors **162**, **164**, **166**, **168** by sensing card select lines CD**0**, CD**1** and configures itself to read files from the inserted card using the pin interface of FIG. **5** corresponding to the card type.

The IDE converter chip **140** executes various routines to perform handshaking with the flash-memory cards and accept data, either serially or in parallel. The data is buffered and then sent either to host PC **20** through IDE connector **146** or to removable mass storage **170**. The IDE converter chip **140** generates the appropriate signals to transfer the data to host PC **20**. The IDE converter chip **140** also generates the control signals for removable mass storage **170**, allowing the image data read from the flash-memory card to be written to removable disk **176**. Removable disk **176** could be a standard or a high-density floppy diskette, a tape drive, a write-able CD-R/W disk, or other proprietary media such as LS120 by Imation of Oakdale, Minn., or ZIP drives by Iomega Corp. of Roy, Utah.

Each of the flash-memory cards in connectors **162**, **164**, **166**, **168** can be assigned a different drive letter by the operating system, such as E:, F:, G:, and H:. Removable mass storage **170** can also be assigned a drive letter.

When Flash reader **180** is not attached to host PC **20**, image files may still be copied to removable mass storage **170**. Flash reader **180** may be carried along on a trip by the user, allowing the user to download image files to removable disk **176**. Since removable disk **176** ordinarily has a much higher capacity than the flash-memory cards, many pictures may be captured when no access to host PC **20** is available. Flash reader **180** can be provided with battery power or with its own AC converter. Optionally an LCD display can be used to preview file names and pictures.

Flash reader **180** is provided with a simple user interface, including light-emitting diode LED **178** and button **179**. When the user inserts a flash-memory card into one of connectors **162**, **164**, **166**, **168**, and removable disk **176** is inserted into removable mass storage **170**, the user presses button **179**. This activates the IDE converter chip **140**, which determines which of connectors **162**, **164**, **166**, **168** has a memory card inserted, and copies the image files to removable mass storage **170**. LED **178** can be programmed to blink during the copying process, and remain lit when the copying is complete, or vice-versa. This provides a simple visual indication to the user of the copying progress. Errors can be indicated with additional LED indicator lamps, or other blinking arrangements or colors.

IDE Converter Chip **140** FIG. **16** is a diagram of the IDE converter chip **140** for the flash-memory reader. The IDE converter chip **140** can be implemented as a commercially available micro-controller chip that is programmed to read and write I/O pins that are connected to the flash-memory-card connectors and the IDE interface. Several different control and transfer routines are written and programmed into RAM/ROM **194**. CPU **192** then executes these routines. A high-level scanning routine can sense when a flash-memory card is inserted. CPU **192** can then begin execution of another routine specific to that type of flash-memory card. Transfer and handshake sub-routines can then be called.

General-purpose input-output GPIO **199** provides registers or I/O ports that drive external I/O pins of the IDE converter chip **140**, or read the logic-levels or voltages on input pins to the IDE converter chip **140**. CPU **192** can read registers in GPIO **199** that are written by control signals that are coupled to I/O pins of the IDE converter chip **140** from connectors **162**, **164**, **166**, **168**. Control signals to the flash-memory cards can be switched high or low by writing a 1 or a 0 to a register for that control signal in GPIO **199**.

Timers **196** are useful for asserting control signals for a required amount of time. For example, a control signal may need to be asserted for a specified number of microseconds. CPU **192** can write a 1 to a register in GPIO **199** and start a timer in timers **196**. Timer **196** can sent an interrupt to CPU **192** when the specified time has elapsed, or CPU **192** can continuously or periodically poll timers **196** to determine when the specified time has elapsed. Then CPU **192** can write a 0 to the register in GPIO **199**, causing the control signal to transition from 1 to 0.

Shifter **198** is connected to the data and clock signals from connectors **164** (not shown), **168**. When data is read from the flash-memory card, a clock is pulsed to synchronize the data transfer. Shifter **198** clocks in one bit (serial) or word (parallel) of data for each clock pulse. A cyclical-redundancy-check (CRC) can be performed on the data to detect errors. CPU **192** can request re-transmission of data from the flash-memory card when an error is detected.

Data read by shifter **198** can be sent over internal bus **190** to be stored in a buffer in RAM/ROM **194**. Later, CPU **192** can execute a routine to transfer this data from RAM/ROM **194** to IDE interface **200**. IDE interface **200** then transmits the data over an external IDE link to a host PC. When a removable mass storage is present, some of the I/O pins from GPIO **199** can connect to the removable mass storage, or a separate disk controller can be included on IDE converter chip **140**.

As is well known, IDE interface only supports one drive per connector. Accordingly, in a system and method in accordance with the present invention, special IDE commands must be provided to allow the interface to be expanded. Typically, there are two slots in a PC, a Master slot and a Slave slot. Accordingly, in a preferred embodiment, two new commands from the CPU **192** are needed, a first command to awaken the device by the converter chip and a second command to identify the device.

The first command which awakens a device such as a CompactFlash+SmartMedia+MemoryStick+MultiMediaCard+Secure Digital Card reader would be described as follows:

—0 nn 0 0 0 0 mm 0×FE where:
—nn is set to 1 to awaken the device and 0 to make the device go to sleep (by default it would be asleep). This can be achieved by asserting a pin on the chip to be low at power up so it would stay inactive until it sees the "wake-up" command.
—mm is 0×E0 if the device is connected as Master and 0×F0 it is a Slave.

The second command for reading/writing to the RAM/ROM 194 loads a plurality of registers as follows:

—0 nn y 0 0 0 mm 0×FD where:
—nn is the number of bytes to write/read
—y is 1 for read and 0 for a write
—mm is 0×E0 if the device is connected as Master slot and 0×F0 if the device is connected as a Slave slot.

Accordingly, through the present invention, the Master and Slave slots are expanded to handle multiple devices via the IDE converter.

Advantages of Improved Flash Reader for Reading Several Types of Flash-Memory Cards with or without a PC

A universal adapter for flash-memory cards accepts cards of several different formats. The adapter accepts SmartMedia, MultiMediaCard, Secure Digital, and Memory Stick cards. The flash-card reader with a single slot accepts any format card using the adapter. Special detection logic on the flash reader distinguishes between the many flash-card formats. The low-cost passive adapter does not need an expensive converter chip. A multi-format reader is ideal for use with a PC. However, a stand-alone flash reader can copy image files from flash cards without a PC. Additionally, preparation of media for use in devices (format and erase operations) can be done using this reader.

A universal adapter is constructed using the CompactFlash card form factor. A reader that reads CompactFlash cards can then read any of the other flash-memory cards that plug into the CompactFlash adapter. The adapters are simple, inexpensive passive adapters without a conversion chip.

The disclosed pin mapping from the smaller flash-card formats to CompactFlash allows for easy detection of the type of flash-memory card inserted into the adapter. Detection of the type of flash-memory card is thus performed automatically by electronic detection by the CompactFlash reader. The CompactFlash reader is modified to perform this card-type detection. Signal conversion such as serial-to-parallel is performed by the CompactFlash reader rather than by the adapter. Adapter costs are reduced while CompactFlash reader cost is increased only slightly. The CompactFlash reader can use a single CompactFlash slot to read multiple flash-card types, including SmartMedia, MultiMediaCard, Secure Digital, Memory Stick, and CompactFlash.

Alternate Embodiments of Improved Flash Reader for Reading Several Types of Flash-Memory Cards with or without a PC

Several other embodiments are contemplated by the inventors. Different flash-card formats can be supported such as Smart Cards, and more or less than the four slots shown in the multi-card flash reader can be included. Other adapters can be used for newer flash formats for the single-slot CompactFlash reader. Any device that needs Control Bus, Clock, Data Bus and Address Bus can be designed to fit into this slot. Examples of such devices include (but are not limited to) DSL Modems, Fingerprint security devices, Miniature Hard disks, Digital Cameras, Video Cameras etc.

While the invention has been described as connecting to a personal computer PC host, the host may also be an Apple computer such as the iMAC or G3. The host may also be a SUN computer or any host computer using IDE interfaces. The invention can also apply to Personal Digital Assistants (PDAs) such as by Palm Computer or other handheld appliances, such as a Cell phone with IDE capability.

The term "CompactFlash reader" has been used for simplicity, since digital images are often read from the flash-memory card and then written to the PC. However, the CompactFlash reader is capable of reading files from the PC or from another flash-memory card and writing the file to the flash-memory card. Thus the CompactFlash reader is really a reader/writer.

In a second embodiment, the CompactFlash reader is a stand-alone device that can operate without a PC. A removable disk media such as a R/W CD-ROM is included. Images from the flash-memory card are copied to the removable disk media by the CompactFlash reader. A simple interface is used; such as having the user press a button to initiate image transfer.

In other alternate embodiments, the CompactFlash reader/multi-flash reader can be designed into a self-hosted appliance such as an MP3 player or a keyboard or a monitor or a stereo appliance. Additionally, the CompactFlash/multi-flash reader can also be designed into handheld data collection scanner devices. The CompactFlash/multi-flash reader can also be designed into personal digital assistant devices, pocket personal computer devices that use, for example, Microsoft Palm operating systems. The compact Flash/multi-flash reader can also be designed into hand terminal devices, personal communicator devices, advanced two-way pager devices, audio recorder and player devices.

In addition, the compact Flash/multi-flash could be designed into monitoring devices for various purposes. The devices include, but are not limited to, any device which requires a PC or paper readout, projector devices, industrial computer devices, printer devices, human input devices, medical devices and digital picture frame devices. These monitoring devices, for example, could be pacemakers, fetal monitors, insulin monitors, chemical monitors, seismic monitors, or the like.

Description of Active Adapter Chip for use in a Flash Card Reader

Although the above-identified CompactFlash readers operate effectively for the stated purpose, they cannot be utilized effectively in certain circumstances. The flash readers only allow for interface to USB on the output side and therefore cannot act as a translator between other interfaces such as IDE, CompactFlash or PCMCIA interfaces. In addition, the conventional method for storing the memory

necessarily means that the some of the slots are inverted. A system and method in accordance with the present invention provides an active adapter that overcomes the above-identified problems.

Universal Active Adapter

FIG. **17** shows a CompactFlash reader system **242** that reads SmartMedia **245**, MultiMediaCard **241**, Secure Digital **243**, and Memory Stick flash-memory cards **247** on the input side and interfaces to CompactFlash **249**, IDE **251** and PCMCIA **253** on an output side. In a preferred embodiment, the CompactFlash reader **242** has an opening or slot with a 50-pin connector that accepts a CompactFlash card **24***a*. An active adapter **240** performs handshaking with a CompactFlash card **24***a* and performs data transfer. The active adapter **240** also controls the interface to the host PC, allowing image files to be transferred to the PC from any of the CompactFlash, IDE interface. Accordingly, the active adapter **240** in accordance with the present invention can read a variety of flash memory cards.

CompactFlash reader **242** can also read other kinds of flash-memory cards. For example, active adapter **240** allows Memory Stick card **247** to be read. Active adapter **240** has an opening that Memory Stick card **247** fits into, while active adapter **240** itself fits into 50-pin connector, since active adapter **240** has the same form factor as a CompactFlash card.

The SmartMedia card can also be read by CompactFlash reader **242**, using active adapter **240**. Likewise, MultiMediaCard or Secure Digital card can be read using active adapter **240**. The active adapter **240** acts as translation between flash media and the plurality of interfaces. FIG. **18** is a table showing the translator in between the flash media and the plurality of interfaces. To describe the features of the active adapter chip **240**A, refer now to the following.

Active Adapter Chip **240**A

FIG. **19** is a block diagram of active adapter chip **240**A in accordance with the present invention. As before mentioned, the active adapter **240** is designed to connect a Memory Stick, SmartMedia, MMC or SD card to a CF slot. On an input side, the active adapter chip **240**A includes a test port **250**, an EEPROM interface **252**, a flash interface **254**, a Memory Stick interface **256** and a clock generator **258**. A processor **260** is coupled to all interfaces **252**, **254** and **256** via a bus **261**. A mask ROM **264** and RAM **266** are also coupled to the bus **261**. On an output side, timers **268**, UART **270**, IRQ **272**, GPIO **274** and a CF, IDE, PCMCIA interface **276** are coupled to the bus **261**. The features of the active adapter chip **240**A will be described herein below.

Input Side

MMC/SD Memory Stick Interface **256**

This interface provides support for MMC/SD and Memory Stick cards. The MultiMediaCard (MMC), Secure Digital Card (SD Card) and MemoryStick are serial access devices. These devices typically require in-bound/out-bound data to be appended with CRC information. The processor provides support in hardware to generate the CRC and to convert serial to parallel and parallel to serial bit streams. A programmable clock speed is provided to set the clock speed based on the media's capabilities.

EEPROM Interface **252**

This port is used to read a serial EEPROM that contains programs for the internal processor.

CompactFlash/Smart Media Interface **254**

This is the port for connecting a parallel device such as CompactFlash or SmartMedia cards. ECC generation and checking is provided for SmartMedia.

Clock Generator **258**

This is the oscillator for the chip's internal clock.

UART Port **270**

The UART port supports 7200 to 115.2K baud. Is useful as a debug port and can also be used to access the EEPROM for reads/writes from the serial port.

Output Side

Timers **268**

The timers are used for time-dependent functions. For example, when power is turned on to a flash card there must be a delay before the card is accessed.

GPIO **274** and IRQ **272**

The GPIOs **274** and IRQ **172** are general-purpose input/output pins. They are used to control various Flash Card functions such as turning power on and off, detecting when a card is plugged in, detecting if a card is write protected, etc. For example, GPIO {11:10} can be used to generate an interrupt to the internal processor when there is change of state on one of these pins. This is used to detect the removal of a flash card.

CF/PCMCIA/IDE Interface **276**

This interface is used to connect to a CompactFlash, PCMCIA, or IDE port. Compact Flash is a subset of PCMCIA, the only real difference being the CompactFlash uses a smaller connector than PCMCIA. IDE is the standard disk connection inside a PC. CompactFlash/PCMCIA or IDE mode is selected when the chip is reset. If—OE is low during reset then IDE mode is selected.

Processing System (Processor **260**, and ROM **264** and RAM **264**)

Processor **260**

The processor (preferably a 16-bit processor) along with the RAM and ROM controls the interface **276**. The processor **260** detects the type of flash card plugged into the CF/Smart Media or MMC/SD/Memory Stick ports, configures itself accordingly and then translates commands received on the CF/PCMCIA/IDE interface **260** and passes them to the attached flash card.

Pin Mapping

FIG. **20** is a table of pin mappings for the SmartMedia, MMC/SD, and Memory Stick to CompactFlash adapters. The pin numbers for the smaller interfaces for SmartMedia, MMC/SD, and Memory Stick are not shown but can be in any order or designation. The adapter connects the proper pin on the smaller interface to the CompactFlash pin number shown in FIG. **20**. Simple wiring such as individual wires, flat cables, printed-circuit board (PCB), or wiring traces can be used.

The ground pins on the smaller interfaces are connected to CompactFlash pins **1** and **50**. Power pins are connected to CompactFlash pins **13**, **38**. Pins **25**, **26** are the card detect signals for CompactFlash, which the adapters connect to the card-detect signals on all smaller interfaces.

The CompactFlash connectors use pins **2**–**6**, **21**–**23**, **27**–**31**, and **47**–**49** for the 16-bit parallel data bus to the CompactFlash card. Pins **8**, **10**–**12**, and **10**–**20** form a separate 11-bit address bus. The separate data and address buses provide for rapid random addressing of CompactFlash

cards. Other control signals include pins **7**, 32 byte enables, pin **9** output enable, pin **36** write enable, interrupt pin **37**, reset pin **41**. Several pins in the 50-pin interface are not connected.

The smaller SmartMedia interface also has a parallel data bus of 8 bits. These are mapped to pins **2**–**6**, and **21**–**23** of the CompactFlash interface to match the CompactFlash D0:7 signals. While no separate address bus is provided, address and data are multiplexed. Control signals for latch enables, write enable and protect, output enable, and ready handshake are among the control signals. Output Enable (OE) and Write Enable (WE) are mapped to the same function pins **9**, **36** of the CompactFlash interface. The total number of pins in the SmartMedia interface is 22.

The Memory Stick and MMC/SD flash-memory-card interfaces are smaller still, since parallel data or address busses are not present. Instead, serial data transfers occur through serial data pin DATAIO, which is mapped to pin **17** (A**3**). Data is clocked in synchronization to clock SERCLK on pin **18**. A command signal CMD or BITSET occupies pin **20** (A**0**). The MMC/SD and Memory Stick interfaces require only 6 pins plus power and ground.

Detection logic in the active adapter chip **240**A reads card-select pins CD**0**, CD**1** to detect the presence of a flash-memory card. When a new card is present, detection logic then reads pins CE**1**, CE**2** as inputs to determine the card type. The wiring inside the adapter and the card's behavior determines whether CE**1**, CE**2** are pulled low or pulled high by the active adapter chip **240**A.

Advantages of the Active Adapter Chip for use in a Flash Card Reader

An active adapter chip for flash-memory cards in accordance with the present invention accepts cards of several different formats. The active adapter chip accepts SmartMedia, MultiMediaCard, Secure Digital, and Memory Stick cards.

The active adapter is constructed using the CompactFlash card form factor. A reader that reads CompactFlash cards can then read any of the other flash-memory cards that plug into the CompactFlash adapter.

The disclosed pin mapping from the smaller flash-card formats to CompactFlash allows for easy detection of the type of flash-memory card inserted into the adapter. Detection of the type of flash-memory card is thus performed automatically by electronic detection by the CompactFlash reader. Signal conversion such as serial-to-parallel is performed by the CompactFlash reader rather than by the adapter. Adapter costs are reduced while CompactFlash reader cost is increased only slightly. The CompactFlash reader can use a single CompactFlash slot to read multiple flash-card types, including SmartMedia, MultiMediaCard, Secure Digital, Memory Stick, and CompactFlash and can also interface on the output side to a plurality of standards, including but not limited to CF, MMD/SC, IDE and PCMCIA standards.

Alternate Embodiments for Active Adapter Chip for use in a Flash Card Reader

The inventors contemplate several other embodiments. Different flash-card formats can be supported such as Smart Cards, and more or less than the four slots shown in the multi-card flash reader can be included. Any device that needs Control Bus, Clock, Data Bus and Address Bus can be designed to fit into these slots. Examples of such devices include (but are not limited to) DSL Modems, Fingerprint security devices, Miniature Hard disks, Digital Cameras, Video Cameras, printers and the like.

While the invention has been described as connecting to a personal computer PC host, the host may also be an Apple computer such as the iMAC or G3. The host may also be a SUN computer, or any host computer using a variety of interfaces. The invention can also apply to personal digital assistants (PDAs) such as by Palm Computer, printers or other handheld appliances, such as a cell phone with a variety of interface capabilities.

The term "CompactFlash reader" has been used for simplicity, since digital images are often read from the flash-memory card and then written to the PC. However, the CompactFlash reader is capable of reading files from the PC or from another flash-memory card and writing the file to the flash-memory card. Thus the CompactFlash reader is really a reader/writer.

In other alternate embodiments, the CompactFlash reader/multi-flash reader can be designed into a self-hosted appliance such as an MP3 player, printer, or a keyboard or a monitor or a stereo appliance. Additionally, the CompactFlash/multi-flash reader can also be designed into handheld data collection scanner devices. The CompactFlash/multi-flash reader can also be designed into personal digital assistant devices, pocket personal computer devices that use, for example, Microsoft Palm operating systems. The compact Flash/multi-flash reader can also be designed into hand terminal devices, personal communicator devices, advanced two-way pager devices, audio recorder and player devices.

Description of Memory Module which Includes a Form Factor Connector

A plurality of flash media are coupled to a single form factor connector to provide a module, i.e., referred to as a SmartStack module that can be coupled directly to the device. The SmartStack module does not include a controller and is controlled from the host side. The form factor connector would typically be a CompactFlash (CF) form factor or some other form factor that are used in a variety of devices. The SmartStack memory module in a preferred embodiment includes a write protect switch that will allow for certain portions of the memory within the SmartStack module not to be written to. In addition, a portion of the flash memory will be allocated to the secure area for storing information to implement various forms of security. Another portion of the flash memory is allocated to store optional biometric information such as a user's fingerprint or retinal scan information, etc.

To more fully describe the present invention, refer now to the following description in conjunction with accompanying figures. FIG. **21** illustrates a SmartStack module **3100**. The SmartStack module **3100** comprises a plurality of memory devices (i.e., flash chips **3102***a*, **3102***b* through **3102***n*) coupled to a connector **3104**. In a preferred embodiment, the flash chips are coupled together such that there is redundancy for each section.

In a preferred embodiment the SmartStack module would have the same form factor as a CompactFlash (CF) card. The module could then be plugged into any CF slot. FIG. **22** illustrates examples of the kinds of applications that can utilize the SmartStack module **3100**, such as a flash reader **3202**, digital camera **3204** or MP3 player **3206**. In a preferred embodiment, only SmartStack module **3202** based CF readers can read/write to SmartStack media, and inserting a SmartStack module into standard CF readers will not damage the SmartStack. As is seen, the SmartStack module does not include a controller and is controlled from the host side. Since the module itself is devoid of any controller it can be expanded easily to add additional memory.

Card Detection

FIG. **23** is a table which illustrates how a particular card will be detected by a device. In this embodiment, when the SmartStack module (i.e., SmartStack NAND or SmartStack NOR) is plugged into the slot, the card detect pins (CD**1** and CD**2**) will be low. For compatibility with a device that can read a SmartStack module card, the card enable pins (CE**1** and CE**2**) will also be low. As is also seen, the other memory modules will have a different pin configuration for detection.

Addressing

FIG. **24** is a table that illustrates addressing of the SmartStack module. In a preferred embodiment, the SmartStack module will be programmed in a manner that is similar to a conventional memory module. The only difference will be the chip selects.

FIG. **24**A illustrates the relationship between the SmartStack module address lines (S**0** . . . S**3**) and their equivalent pins in a CompactFlash card.

Security and Biometric Information

FIG. **25** illustrates a SmartStack module **3300** which includes the write protect mechanism **3302**, security area **3304** and biometric area **3306**. The write protect mechanism can be locked or unlocked to allow for writing to the module. The write protect mechanism in a preferred embodiment may be read by software to prevent writing in the user area. It may be necessary to allocate space for security and biometric on each of the individual flash media, in which case the same table will be used to create this information. As is seen in this embodiment, the secure area **3304** and biometric area **3306** are allocated on **3102***a*'. One of ordinary skill in the art recognizes that the areas **3302** and **3304** could be located in any or all of the flash chips **3102***a*'–**3102***n*' and that would be within the spirit and scope of the present invention that which illustrates the setting of a secure area of data for the SmartStack module. For providing a secure area in the SmartStack module, in a preferred embodiment the following method will be followed: the first two bytes, byte **0** and byte **1**, will be set to C3 B6. The next byte, byte **2**, defines the function. In addition, byte **5** (block status flag) will always be set to 0×F0 (or 0×0F) to indicate a failed block so that an operating system or firmware will not write over it accidentally.

An additional improvement for performance would be to add random access memory (RAM) to the stack. FIG. **27** illustrates adding a RAM **3402** to SmartStack module **3400** to improve performance. By adding the RAM **3402** to the module **3400**, data can be cached thereto thereby allowing for faster access to data in the module.

Additionally the SmartStack module can be designed to function like daughter boards on a base board so the capacity can be modularly increased. The SmartStack module can also be designed such that you can plug one card at the end of the previous one to form a chain (or daisy chain).

FIG. **28** illustrates daisy-chaining a plurality of SmartStack modules **500** and **502** in accordance with the present invention. Accordingly, in this embodiment, one SmartStack module **500** would include a female connector **506** on one end and a male (expansion port) connector **508** on the other to allow more cards to be plugged in. In an alternate embodiment, the expansion card can be itself devised to have several expansion ports (female connectors) into which users can plug in SmartStack modules. The SmartStack module can optionally enable the user to have the capability of being able to review the pictures before committing it (saving it) to the flash media itself.

FIG. **29** illustrates a SmartStack module **600**, which is an expansion bay. In this embodiment, additional SmartStack modules can be plugged into male connection slots **602** and the female connector **604** would connect to a SmartStack enabled CompactFlash Host.

Multimode Controller for Intelligent and "Dumb" Flash Cards

Most flash card system controllers can only work together with one type of flash medium. FIG. **30** illustrates a system that is adaptable to a single media type. However, as is known to the inventor and described above, in some cases some controllers may work with multiple media types at the same time.

Host computer **4000** may be any of a variety of computers, such as a PC, notebook, PDA, etc., having an interface connection **4001** that connects to controller IC **4010**. For purposes of simplicity and clarity, the connection details are not shown. As described earlier, the interface connection may be any of a wide variety of types, such as IDE, USB, or (not shown above) Ethernet. Or it may be a system bus (PCI, etc.), or any other kind of suitable network interface or connectivity offered by computer **4000**. Said interface is converted by controller IC **4010** into an interface **4011** to the flash medium **4020**. Many aspects of that interface **4011** (and possible adapters, not shown here for clarity) have been described in great detail in previous sections, above.

Host computer **4000** also typically has driver software **4002**, and adapter chip **4010** contains firmware **4012**. Flash medium **4020** typically may consist of a controller section **4021** and a flash section **4022**. In most cases, these sections are at least two separate ICs, although in some cases they may be integrated into one IC. However, in all cases, there is a significant added cost for the controller section, whether it comprises a separate chip or is integrated into a single IC with the flash.

Typically, the purpose of controller **4021** is to present a flawless medium to the system, in a specific format, so the computer **4000** sees an error-free storage medium **4020**, rather than a flash **4022** that may have certain defects that must be mapped away.

FIG. **31** shows an improved flash medium **4020***b*. Flash medium **4020***b* still has a flash section or IC **4022**, but the controller section **4021** has been removed. Shown now in detail is a medium ID **4030**, some aspects of which have been discussed in earlier sections above, and which in some cases may be split between the flash medium and the media adapter cards, as also described earlier. That medium ID **4030** includes in some cases certain basic specifications of the medium, such as the memory type, the total capacity, etc. Originally, the controller **4021** (FIG. **30**) was used to provide that kind of information; however, as discussed just above, the primary reason for including a controller section in a flash medium is for error correction. This task is now shifted either to firmware **4012***b* of the host computer, which now, on top of its normal access section software, also manages error correction and bad block mapping of chip(s) **4022** and stores those parameters in flash medium **4020***b* itself. Or in some cases, this function may be shifted to driver software **4002***b* in the host computer **4000**.

Often this error mapping and other functions may be handled in combination between those two software elements (firmware **4012***b* and driver software **4002***b*), or in some cases it may be shifted entirely to firmware **4012***b*, which allows the driver software **4002** to remain a standard removable medium driver rather than including specialized firmware. Shifting control entirely to firmware **4012***b* allows

for transparent use of the flash, much as the original controller **4021** (FIG. **30**) did. Thus an operating system would not be able to distinguish one from the other, and no special drivers, patches, etc., would have to be installed by the user.

Identification **4030** makes use of those pins discussed in the sections' above (see FIG. **5**, for example), and in all those cases discussed above, a mechanical-electrical medium adapter may be used on bus **4011** for different electromechanical connection interfaces, etc.

FIG. **32** shows various implementations of ID **4030**. For example, ID **4030***a* uses simple pull-ups and pull-downs, as discussed earlier. ID **4030***b* uses, rather than simple pull-ups and pull-downs, voltage dividers, in this example consisting of R**2**/R**3** and R**4**/R**5**. By using voltage dividers, a limited number of pins, such as, for example, two, can be stretched into offering 16 or even more different types of cards or IDs, based on the fact that, rather than one bit per pin (high or low), multiple voltage levels (and hence multiple bits) per pin can now be supported, using voltage dividers, and therefore many more card combinations can be identified through a limited number of pins. On the controller side, comparators may be used to regenerate digital signals (not shown for clarity).

ID **4030***c* achieves the same result by having a small E^2 programmable ROM as a digital ID. This could be a mask program or E^2-type serial memory, which is available very inexpensively. The E^2 could be programmed at the factory or in the field through firmware **4012***b*. Many types of low pin count serial buses are known to the inventor and to those skilled in the art (such as Single Wire™ by Dallas Semiconductor, I^2C etc.), counting from 1–4 pins including power in some cases. The advantage of using the E^2 would be, for example, to allow use of a flash chip **4022** that even has a bad boot sector, because a new boot sector address could be incorporated into **4030***c*, rather than having to rely on the main storage **4022** to be error free.

As the industry moves to higher and higher single-chip capacity, the chances of having bad sectors in the boot section increase. By moving the boot sector address into an auxiliary device, such as ID **4030***c*, the yield of usable chips **4022** can be dramatically increased, and therefore costs can be further reduced.

Also, elimination of the controller **4021** helps to further reduce the cost of medium **4022**. By having a combined firmware **4012***b* that can handle both media cards **4022** with controllers of all formats discussed above and of others not discussed, as well as controller-less media cards such as **4020***b*, with an ID **4030**, backward compatibility is guaranteed in the market.

Although the present invention has been described in accordance with the embodiments shown, one of ordinary skill in the art will readily recognize that there could be variations to the embodiments and those variations would be within the spirit and scope of the present invention. Accordingly, many modifications may be made by one of ordinary skill in the art without departing from the spirit and scope of the appended claims.

What is claimed is:

1. A controller chip comprising:

an interface mechanism capable of receiving flash storage systems with controllers and flash storage systems without controllers, a flash storage system to be coupled to a computer system;

a detector to determine whether the flash storage system includes a controller for error correction; and

a flash adapter to interface the computer system with the flash storage system, the flash adapter comprising:

a first interface to be coupled to the computer system;

a second of interface to be coupled to the flash storage system, wherein the flash storage system comprises a flash section and at least a medium ID; and

a firmware in the flash adapter, in an event where the flash storage system does not have a controller for error correction, to perform operations to manage error correction of the flash section in the flash storage system that is coupled to the flash adapter by the second interface, including bad block mapping of the flash section.

2. The controller chip of claim **1**, wherein the medium ID contains specifications of the flash storage system.

3. The controller chip of claim **2**, wherein the flash adapter further comprises at least another portion of the medium ID.

4. The controller chip of claim **2**, wherein the medium ID comprises a pull-up resistor and a pull-down resistor.

5. The controller chip of claim **2**, wherein the medium ID further comprises a voltage divider.

6. The controller chip of claim **2**, wherein the medium ID further comprises an EEPROM device to store the specifications of the flash storage system.

7. A method comprising:

using a controller chip to interface a flash storage system with or without a controller to a computing device, the controller chip comprising a flash adapter, wherein the flash storage system comprises a flash section and at least a medium ID;

determining whether the flash storage system includes a controller for error correction; and

in an event where the flash storage system does not have a controller for error correction, using firmware in the flash adapter to perform operations to manage error correction of the flash section, including bad block mapping of the flash section in the flash storage system that is coupled to the flash adapter section.

8. The method of claim **7**, further comprising: storing specifications of the flash storage system in the medium ID.

9. The method of claim **7**, further comprising updating the specifications in the medium ID during bad block mapping of the flash section, wherein the medium ID comprises one or more EEPROM devices to store the specifications.

10. The method of claim **7**, further comprising examining the medium ID to identify a type of the flash storage system, wherein the medium ID comprises at least one of a pull-up resistor, a pull-down resistor, and a voltage divider.

11. A system comprising:

a computing device;

a flash storage system comprising a flash section and at least a portion of a medium ID; and

a controller chip coupled between the computing device and the flash storage system to interface the flash storage system to the computing device, the controller chip comprising an interface mechanism capable of receiving flash storage systems with controller and controllerless flash storage systems, a detector to determine whether the flash storage system includes a controller for error correction and a flash adapter which comprises firmware to perform, in an event where the flash storage system does not have a controller for error correction, operations to manage error correction of the flash section, including bad block mapping of the flash section in the flash storage system that is coupled to the flash adapter section.

12. The system of claim **11**, wherein the medium ID contains specifications of the flash storage system.

13. The system of claim **12**, wherein the flash adapter further comprises at least another portion of the medium ID.

14. The system of claim **12**, wherein the medium ID comprises a pull-up resistor and a pull-down resistor.

15. The system of claim **12**, wherein the medium ID comprises a voltage divider.

16. The system of claim **12**, wherein the medium ID comprises an EEPROM device to store the specifications of the flash storage system.

17. The controller chip of claim **1**, wherein the flash adapter further comprises a plurality of interfaces for receiving a plurality of flash storage systems.

18. The controller chip of claim **1**, wherein the bad block mapping includes addressing a new boot sector to allow use of the storage system with a bad boot sector.

19. The method of claim **7**, wherein the flash adapter further comprises a plurality of interfaces for receiving a plurality of flash storage systems.

20. The method of claim **7**, wherein the bad block mapping includes addressing a new boot sector to allow use of the storage system with a bad boot sector.

21. The system of claim **11**, wherein the flash adapter further comprises a plurality of interfaces for receiving a plurality of flash storage systems.

22. The controller chip of claim **11**, wherein the bad block mapping includes addressing a new boot sector to allow use of the storage system with a bad boot sector.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,162,549 B2
APPLICATION NO. : 10/264466
DATED : January 9, 2007
INVENTOR(S) : Sreenath Mambakkam et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In Column 1,
Line 17, add the following text: -- Ser. No. 10/039,685 and Ser. No. 10/063,021 are continuations-in-part of Ser. No. 09/610,904, filed on Jul. 6, 2000, now U.S. Pat. No. 6,438,638 entitled "Flashtoaster for Reading Several Types of Flash-Memory Cards With or Without a PC." --

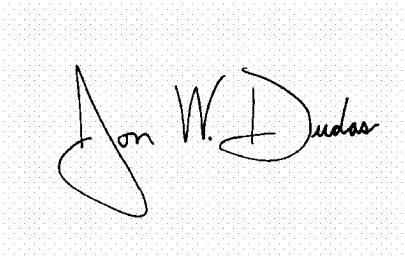
In Column 29,
Line 65, replace "error correction;" with -- error correction,--

In Column 29,
Lines 59-67 should be formatted as follows:
-- 1. A controller chip comprising:
an interface mechanism capable of receiving flash storage systems with controllers and flash storage systems without controllers, a flash storage system to be coupled to a computer system; a detector to determine whether the flash storage system includes a controller for error correction, and a flash adapter to interface the computer system with the flash storage system, the flash adapter comprising: --

In Column 30,
Line 2, replace "a second of interface" with -- a second interface --

Signed and Sealed this

Thirteenth Day of March, 2007



JON W. DUDAS
Director of the United States Patent and Trademark Office

ADDENDUM B

U. S Constitution

Article III

Section 1.

The judicial power of the United States, shall be vested in one Supreme Court, and in such inferior courts as the Congress may from time to time ordain and establish. The judges, both of the supreme and inferior courts, shall hold their offices during good behaviour, and shall, at stated times, receive for their services, a compensation, which shall not be diminished during their continuance in office.

Section 2.

The judicial power shall extend to all cases, in law and equity, arising under this Constitution, the laws of the United States, and treaties made, or which shall be made, under their authority;--to all cases affecting ambassadors, other public ministers and consuls;--to all cases of admiralty and maritime jurisdiction;--to controversies to which the United States shall be a party;--to controversies between two or more states;--between a state and citizens of another state;--between citizens of different states;--between citizens of the same state claiming lands under grants of different states, and between a state, or the citizens thereof, and foreign states, citizens or subjects.

In all cases affecting ambassadors, other public ministers and consuls, and those in which a state shall be party, the Supreme Court shall have original jurisdiction. In all the other cases before mentioned, the Supreme Court shall have appellate jurisdiction, both as to law and fact, with such exceptions, and under such regulations as the Congress shall make.

The trial of all crimes, except in cases of impeachment, shall be by jury; and such trial shall be held in the state where the said crimes shall have been committed; but when not committed within any state, the trial shall be at such place or places as the Congress may by law have directed.

Section 3.

Treason against the United States, shall consist only in levying war against them, or in adhering to their enemies, giving them aid and comfort. No person shall be convicted of treason unless on the testimony of two witnesses to the same overt act, or on confession in open court.

The Congress shall have power to declare the punishment of treason, but no attainder of treason shall work corruption of blood, or forfeiture except during the life of the person attainted.

U.S Constitution

Amendment VII

In suits at common law, where the value in controversy shall exceed twenty dollars, the right of trial by jury shall be preserved, and no fact tried by a jury, shall be otherwise reexamined in any court of the United States, than according to the rules of the common law.

U.S. Code
Title 35 - PATENTS
PART III - PATENTS AND PROTECTION OF PATENT RIGHTS
CHAPTER 31—INTER PARTES REVIEW

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§312. Petitions

(a) Requirements of Petition.—A petition filed under section 311 may be considered only if—

(1) the petition is accompanied by payment of the fee established by the Director under section 311;

(2) the petition identifies all real parties in interest;

(3) the petition identifies, in writing and with particularity, each claim challenged, the grounds on which the challenge to each claim is based, and the evidence that supports the grounds for the challenge to each claim, including—

(A) copies of patents and printed publications that the petitioner relies upon in support of the petition; and

(B) affidavits or declarations of supporting evidence and opinions, if the petitioner relies on expert opinions;

(4) the petition provides such other information as the Director may require by regulation; and

(5) the petitioner provides copies of any of the documents required under paragraphs (2), (3), and (4) to the patent owner or, if applicable, the designated representative of the patent owner.

(b) Public Availability.—As soon as practicable after the receipt of a petition under section 311, the Director shall make the petition available to the public.

(Added Pub. L. 106–113, div. B, §1000(a)(9) [title IV, §4604(a)], Nov. 29, 1999, 113 Stat. 1536, 1501A–568; amended Pub. L. 107–273, div. C, title III, §§13105(a), 13202(a)(2), (c)(1), Nov. 2, 2002, 116 Stat. 1900–1902; Pub. L. 112–29, §6(a), (c)(3)(A)(i), Sept. 16, 2011, 125 Stat. 300, 305.)

Amendments

2011—Pub. L. 112–29, §6(a), amended section generally. Prior to amendment, section related to determination of issue by Director.

Subsec. (a). Pub. L. 112–29, §6(c)(3)(A)(i)(I), substituted "the information presented in the request shows that there is a reasonable likelihood that the requester would prevail with respect to at least 1 of the claims challenged in the request," for "a substantial new question of patentability affecting any claim of the patent concerned is raised by the request," and "A showing that there is a reasonable likelihood that the requester would prevail with respect to at least 1 of the claims challenged in the request" for "The existence of a substantial new question of patentability".

Subsec. (c). Pub. L. 112–29, §6(c)(3)(A)(i)(II), substituted "the showing required by subsection (a) has not been made," for "no substantial new question of patentability has been raised,".

2002—Pub. L. 107–273, §13202(c)(1), made technical correction to directory language of Pub. L. 106–113, which enacted this section.

Subsec. (a). Pub. L. 107–273, §13202(a)(2)(A), struck out second sentence which read as follows: "On the Director's initiative, and at any time, the Director may determine whether a substantial new question of patentability is raised by patents and publications."

Pub. L. 107–273, §13105(a), inserted at end "The existence of a substantial new question of patentability is not precluded by the fact that a patent or printed publication was previously cited by or to the Office or considered by the Office."

Subsec. (b). Pub. L. 107–273, §13202(a)(2)(B), struck out ", if any" after "third-party requester".

Effective Date of 2011 Amendment

Amendment by section 6(a) of Pub. L. 112–29 effective upon the expiration of the 1-year period beginning on Sept. 16, 2011, and applicable to any patent issued before, on, or after that effective date, with provisions for graduated implementation, see section 6(c)(2) of Pub. L. 112–29, set out as a note under section 311 of this title.

Pub. L. 112–29, §6(c)(3)(B), (C), Sept. 16, 2011, 125 Stat. 305, provided that:

"(B) Application.—The amendments made by this paragraph [amending this section and section 313 of this title]—

"(i) shall take effect on the date of the enactment of this Act [Sept. 16, 2011]; and

"(ii) shall apply to requests for inter partes reexamination that are filed on or after such date of enactment, but before the effective date set forth in paragraph (2)(A) of this subsection [set out as a note under section 311 of this title].

"(C) Continued applicability of prior provisions.—The provisions of chapter 31 of title 35, United States Code, as amended by this paragraph [amending this section and section 313 of this title], shall continue to apply to requests for inter partes reexamination that are filed before the effective date set forth in paragraph (2)(A) as if subsection (a) [enacting section 319 of this title and amending this section and sections 312 to 318 of this title] had not been enacted."

Effective Date of 2002 Amendment

Amendment by section 13105(a) of Pub. L. 107–273 applicable with respect to any determination of the Director of the United States Patent and Trademark Office that is made on or after Nov. 2, 2002, see section 13105(b) of Pub. L. 107–273, set out as a note under section 303 of this title.

U.S. Code
Title 35 - PATENTS
PART III - PATENTS AND PROTECTION OF PATENT RIGHTS
CHAPTER 31—INTER PARTES REVIEW

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§315. Relation to other proceedings or actions

(a) Infringer's Civil Action.—

(1) Inter partes review barred by civil action.—An inter partes review may not be instituted if, before the date on which the petition for such a review is filed, the petitioner or real party in interest filed a civil action challenging the validity of a claim of the patent.

(2) Stay of civil action.—If the petitioner or real party in interest files a civil action challenging the validity of a claim of the patent on or after the date on which the petitioner files a petition for inter partes review of the patent, that civil action shall be automatically stayed until either—

(A) the patent owner moves the court to lift the stay;

(B) the patent owner files a civil action or counterclaim alleging that the petitioner or real party in interest has infringed the patent; or

(C) the petitioner or real party in interest moves the court to dismiss the civil action.

(3) Treatment of counterclaim.—A counterclaim challenging the validity of a claim of a patent does not constitute a civil action challenging the validity of a claim of a patent for purposes of this subsection.

(b) Patent Owner's Action.—An inter partes review may not be instituted if the petition requesting the proceeding is filed more than 1 year after the date on which the petitioner, real party in interest, or privy of the petitioner is served with a complaint alleging infringement of the patent. The time limitation set forth in the preceding sentence shall not apply to a request for joinder under subsection (c).

(c) Joinder.—If the Director institutes an inter partes review, the Director, in his or her discretion, may join as a party to that inter partes review any person who properly files a petition under section 311 that the Director, after receiving a preliminary response under section 313 or the expiration of the time for filing such a response, determines warrants the institution of an inter partes review under section 314.

(d) Multiple Proceedings.—Notwithstanding sections 135(a), 251, and 252, and chapter 30, during the pendency of an inter partes review, if another proceeding or matter

involving the patent is before the Office, the Director may determine the manner in which the inter partes review or other proceeding or matter may proceed, including providing for stay, transfer, consolidation, or termination of any such matter or proceeding.

(e) Estoppel.—

(1) Proceedings before the office.—The petitioner in an inter partes review of a claim in a patent under this chapter that results in a final written decision under section 318(a), or the real party in interest or privy of the petitioner, may not request or maintain a proceeding before the Office with respect to that claim on any ground that the petitioner raised or reasonably could have raised during that inter partes review.

(2) Civil actions and other proceedings.—The petitioner in an inter partes review of a claim in a patent under this chapter that results in a final written decision under section 318(a), or the real party in interest or privy of the petitioner, may not assert either in a civil action arising in whole or in part under section 1338 of title 28 or in a proceeding before the International Trade Commission under section 337 of the Tariff Act of 1930 that the claim is invalid on any ground that the petitioner raised or reasonably could have raised during that inter partes review.

(Added Pub. L. 106–113, div. B, §1000(a)(9) [title IV, §4604(a)], Nov. 29, 1999, 113 Stat. 1536, 1501A–569; amended Pub. L. 107–273, div. C, title III, §§13106(a), 13202(a)(4), (c)(1), Nov. 2, 2002, 116 Stat. 1900–1902; Pub. L. 112–29, §6(a), Sept. 16, 2011, 125 Stat. 300.)

References in Text

Section 337 of the Tariff Act of 1930, referred to in subsec. (e)(2), is classified to section 1337 of Title 19, Customs Duties.

Amendments

2011—Pub. L. 112–29 amended section generally. Prior to amendment, section related to appeals.

2002—Pub. L. 107–273, §13202(c)(1), made technical correction to directory language of Pub. L. 106–113, which enacted this section.

Subsec. (b). Pub. L. 107–273, §13106(a), reenacted heading without change and amended text generally. Prior to amendment, text read as follows: "A third-party requester may—

"(1) appeal under the provisions of section 134 with respect to any final decision favorable to the patentability of any original or proposed amended or new claim of the patent; or

"(2) be a party to any appeal taken by the patent owner under the provisions of section 134, subject to subsection (c)."

Subsec. (c). Pub. L. 107–273, §13202(a)(4), struck out "United States Code," after "title 28,".

Effective Date of 2011 Amendment

Amendment by Pub. L. 112–29 effective upon the expiration of the 1-year period beginning on Sept. 16, 2011, and applicable to any patent issued before, on, or after that effective date, with provisions for graduated implementation, see section 6(c)(2) of Pub. L. 112–29, set out as a note under section 311 of this title.

Effective Date of 2002 Amendment

Amendment by section 13106(a) of Pub. L. 107–273 applicable with respect to any reexamination proceeding commenced on or after Nov. 2, 2002, see section 13106(d) of Pub. L. 107–273, set out as a note under section 134 of this title.

Estoppel Effect of Reexamination

Pub. L. 106–113, div. B, §1000(a)(9) [title IV, subtitle F, §4607], Nov. 29, 1999, 113 Stat. 1536, 1501A–571, provided for estoppel from challenging certain facts determined during inter partes reexamination under former section 311 of this title and contained a severability provision.

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Title 35 - PATENTS
PART III - PATENTS AND PROTECTION OF PATENT RIGHTS
CHAPTER 31—INTER PARTES REVIEW

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§316. Conduct of inter partes review

(a) Regulations.—The Director shall prescribe regulations—

(1) providing that the file of any proceeding under this chapter shall be made available to the public, except that any petition or document filed with the intent that it be sealed shall, if accompanied by a motion to seal, be treated as sealed pending the outcome of the ruling on the motion;

(2) setting forth the standards for the showing of sufficient grounds to institute a review under section 314(a);

(3) establishing procedures for the submission of supplemental information after the petition is filed;

(4) establishing and governing inter partes review under this chapter and the relationship of such review to other proceedings under this title;

(5) setting forth standards and procedures for discovery of relevant evidence, including that such discovery shall be limited to—

(A) the deposition of witnesses submitting affidavits or declarations; and

(B) what is otherwise necessary in the interest of justice;

(6) prescribing sanctions for abuse of discovery, abuse of process, or any other improper use of the proceeding, such as to harass or to cause unnecessary delay or an unnecessary increase in the cost of the proceeding;

(7) providing for protective orders governing the exchange and submission of confidential information;

(8) providing for the filing by the patent owner of a response to the petition under section 313 after an inter partes review has been instituted, and requiring that the patent owner file with such response, through affidavits or declarations, any additional factual evidence and expert opinions on which the patent owner relies in support of the response;

(9) setting forth standards and procedures for allowing the patent owner to move to amend the patent under subsection (d) to cancel a challenged claim or propose a reasonable number of substitute claims, and ensuring that any information submitted by the patent owner in support of any amendment entered under subsection (d) is made available to the public as part of the prosecution history of the patent;

(10) providing either party with the right to an oral hearing as part of the proceeding;

(11) requiring that the final determination in an inter partes review be issued not later than 1 year after the date on which the Director notices the institution of a review under this chapter, except that the Director may, for good cause shown, extend the 1-year period by not more than 6 months, and may adjust the time periods in this paragraph in the case of joinder under section 315(c);

(12) setting a time period for requesting joinder under section 315(c); and

(13) providing the petitioner with at least 1 opportunity to file written comments within a time period established by the Director.

(b) Considerations.—In prescribing regulations under this section, the Director shall consider the effect of any such regulation on the economy, the integrity of the patent system, the efficient administration of the Office, and the ability of the Office to timely complete proceedings instituted under this chapter.

(c) Patent Trial and Appeal Board.—The Patent Trial and Appeal Board shall, in accordance with section 6, conduct each inter partes review instituted under this chapter.

(d) Amendment of the Patent.—

(1) In general.—During an inter partes review instituted under this chapter, the patent owner may file 1 motion to amend the patent in 1 or more of the following ways:

(A) Cancel any challenged patent claim.

(B) For each challenged claim, propose a reasonable number of substitute claims.

(2) Additional motions.—Additional motions to amend may be permitted upon the joint request of the petitioner and the patent owner to materially advance the settlement of a proceeding under section 317, or as permitted by regulations prescribed by the Director.

(3) Scope of claims.—An amendment under this subsection may not enlarge the scope of the claims of the patent or introduce new matter.

(e) Evidentiary Standards.—In an inter partes review instituted under this chapter, the petitioner shall have the burden of proving a proposition of unpatentability by a preponderance of the evidence.

(Added Pub. L. 106–113, div. B, §1000(a)(9) [title IV, §4604(a)], Nov. 29, 1999, 113 Stat. 1536, 1501A–569; amended Pub. L. 107–273, div. C, title III, §13202(c)(1), Nov. 2, 2002, 116 Stat. 1902; Pub. L. 112–29, §6(a), Sept. 16, 2011, 125 Stat. 302.)

Amendments

2011—Pub. L. 112–29 amended section generally. Prior to amendment, section related to certificate of patentability, unpatentability, and claim cancellation.

2002—Pub. L. 107–273 made technical correction to directory language of Pub. L. 106–113, which enacted this section.

Effective Date of 2011 Amendment

Amendment by Pub. L. 112–29 effective upon the expiration of the 1-year period beginning on Sept. 16, 2011, and applicable to any patent issued before, on, or after that effective date, with provisions for graduated implementation, see section 6(c)(2) of Pub. L. 112–29, set out as a note under section 311 of this title.

CFR
Title 37: Patents, Trademarks, and Copyrights
PART 42—TRIAL PRACTICE BEFORE THE PATENT TRIAL AND APPEAL BOARD
Subpart B—Inter Partes Review

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§42.104 Content of petition

In addition to the requirements of §§42.6, 42.8, 42.22, and 42.24, the petition must set forth:

(a) *Grounds for standing*. The petitioner must certify that the patent for which review is sought is available for *inter partes* review and that the petitioner is not barred or estopped from requesting an *inter partes* review challenging the patent claims on the grounds identified in the petition.

(b) *Identification of challenge*. Provide a statement of the precise relief requested for each claim challenged. The statement must identify the following:

(1) The claim;

(2) The specific statutory grounds under 35 U.S.C. 102 or 103 on which the challenge to the claim is based and the patents or printed publications relied upon for each ground;

(3) How the challenged claim is to be construed. Where the claim to be construed contains a means-plus-function or step-plus-function limitation as permitted under 35 U.S.C. 112(f), the construction of the claim must identify the specific portions of the specification that describe the structure, material, or acts corresponding to each claimed function;

(4) How the construed claim is unpatentable under the statutory grounds identified in paragraph (b)(2) of this section. The petition must specify where each element of the claim is found in the prior art patents or printed publications relied upon; and

(5) The exhibit number of the supporting evidence relied upon to support the challenge and the relevance of the evidence to the challenge raised, including identifying specific portions of the evidence that support the challenge. The Board may exclude or give no weight to the evidence where a party has failed to state its relevance or to identify specific portions of the evidence that support the challenge.

(c) A motion may be filed that seeks to correct a clerical or typographical mistake in the petition. The grant of such a motion does not change the filing date of the petition.

CFR
Title 37: Patents, Trademarks, and Copyrights
PART 41—PRACTICE BEFORE THE PATENT TRIAL AND APPEAL BOARD
Subpart A—General Provisions

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§41.8 Mandatory notices

(a) In an appeal brief (§§41.37, 41.67, or 41.68) or at the initiation of a contested case (§41.101), and within 20 days of any change during the proceeding, a party must identify:

(1) Its real party-in-interest, and

(2) Each judicial or administrative proceeding that could affect, or be affected by, the Board proceeding.

(b) For contested cases, a party seeking judicial review of a Board proceeding must file a notice with the Board of the judicial review within 20 days of the filing of the complaint or the notice of appeal. The notice to the Board must include a copy of the complaint or notice of appeal. See also §§1.301 to 1.304 of this title.

No. 15-1091

United States Court of Appeals for the Federal Circuit

MCM PORTFOLIO LLC,
APPELLANT,

v.

HEWLETT-PACKARD COMPANY,
APPELLEE.

PROOF OF SERVICE

I, Rita L. Hemenway, being duly sworn according to law and being over the age of 18, upon my oath depose and say that: Bateman & Slade, Inc. was retained by Edward P. Heller III, Attorney for Appellant to print this document. I am an employee of Bateman & Slade, Inc.

On **January 20, 2015**, Counsel for Appellant has authorized me to electronically file the foregoing **PRINCIPAL BRIEF FOR APPELLANT** with the Clerk of Court using the CM/ECF System, which will serve via e-mail notice of such filing to counsel for Appellee pursuant to Fed. R. App. P. 25 and Fed. Cir. R. 25(a) and 25 (b).

Additionally, paper copies will be mailed to the principal counsel at the below addresses on the date paper copies are sent to the Court.

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Upon acceptance by the Court of the e-filed document, six paper copies will be filed with the Court, via Express Mail, within the time provided in the Court's rules.

/s/ Rita L. Hemenway
Rita L. Hemenway

CERTIFICATE OF COMPLIANCE

1. This brief complies with the type-volume limitation of Federal Rule of Appellate Procedure 32(a)(7)(B) or Federal Rule of Appellate Procedure 28.1(e).

   X The brief contains 11,474 words, excluding the parts of the brief exempted by Federal Rule of Appellate Procedure 32(a)(7)(B)(iii),or

2. This brief complies with the typeface requirements of Federal Rule of Appellate Procedure 32(a)(5) and the type style requirements of Federal Rule of Appellate Procedure 32(a)(6).

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January 20, 2015

/s/ Edward P. Heller III
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